Experiment 7

Design and implement a synchronous digital system (with an active low asynchronous clear) to detect the non-resetting binary input sequence 1100 or 1000. Use the state table given below as the starting point for your design/implementation.

Design your circuit as a Mealy machine using T flip flops (to be constructed using JK flip flops with asynchronous preset and clear).

Present State	Next State		Output (`Z_BAR`)		Encoding
	X=0	X=1	X=0	X=1	$Q_A Q_B Q_C$
S_0	S_0	S_1	1	1	001
S_1	S_4	S_2	1	1	101
S_2	S_3	S_2	1	1	111
S_3	S_5	S_1	0	1	010
S_4	S_5	S_1	1	1	011
S_5	S_0	S_1	0	1	000

Task: Design/develop the sequence detector's combinational parts.

Deliverable (D1): Next state K-maps, T FF input K-maps and the output K-map. Minimized equations for T FF inputs and for the output. Annotated logic schematic for the sequential circuit (both combinational parts and memory).

Task: Develop a structural VHDL model of the sequential machine using the VHDL models for the TTL ICs SN7476, SN7486 and SN7432. You are allowed two instances of SN7476 and, one instance of each of the other two ICs. VHDL models can be found in `~csci355/Lab7`.

Deliverable (D2): Electronic submission of source code (`make submit`).

Task: Map your VHDL model to a TTL-based physical design for the sequential system.

Deliverable (D3): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D4): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D5): A physical realization of the sequential system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D6): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES