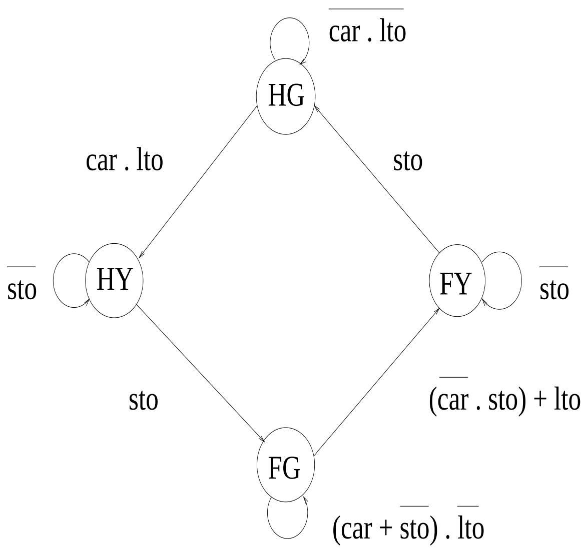
Experiment 9

Design and implement a controller for a traffic light at the intersection of a highway and a farm-road. The behaviour of the controller is as follows. The highway lights remain green as long as there are no cars on the farm-road. When the highway lights have been green for a minimum of ten seconds, a car on the farm-road will cause the highway lights to go yellow for three seconds and then red. Then the farm-road lights will turn green and remain green for a minimum of three seconds. The presence of other cars on the farm-road beyond the three seconds will enable the farm-road lights to remain green for a maximum of ten seconds. The farm-road lights will then go yellow for three seconds and then red.

The controller is to have four states, highway green (`HG`), highway yellow (`HY`), farm-road green (`FG`) and farm-road yellow (`FG`). In state `HG`, the highway lights are green and the farm-road lights are red. In state `HY`, the highway lights are yellow and the farm-road lights are red. In state `FG`, the farm-road lights are green and the highway lights are red. In state `FY`, the farm-road lights are yellow and the highway lights are red. The controller is to have five control signals: `clear_BAR`, `car` , `sto`, `lto` and `clk`. The control signal `clear_BAR` is asynchronous. All other control signals are synchronous. When `clear_BAR` is asserted, the controller resets to state `HG`. When `car` is asserted, a car is present on the farm-road. When `lto` is asserted, a long-delay timer has reached the ten second mark. When `sto` is asserted, a short-delay timer has reached the three second mark.

There are five single-bit inputs and six single-bit outputs. The five inputs correspond to the control signals described earlier. Three of the outputs correspond to the red, green and yellow lights visible from the highway. They are `hw_R, hw_G, hw_Y`. The other three correspond to the red, green and yellow lights visible from the farm-road. They are `fr_R, fr_G, fr_Y`.

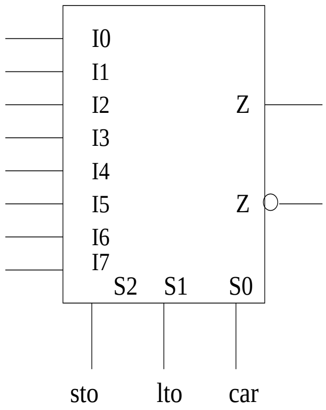
State transitions are shown in the following state diagram.

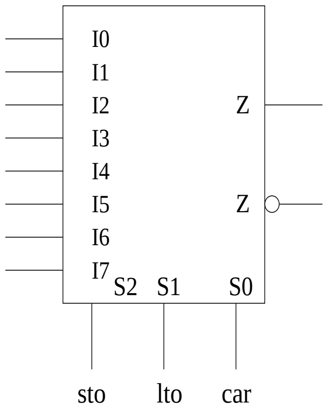


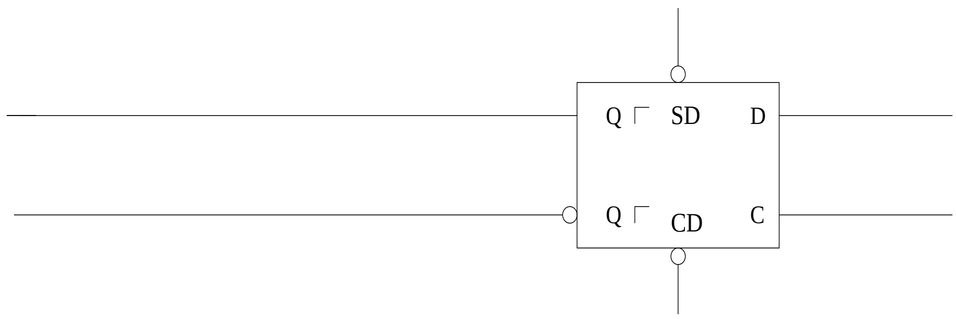
State assignment is shown in the following state assignment table.

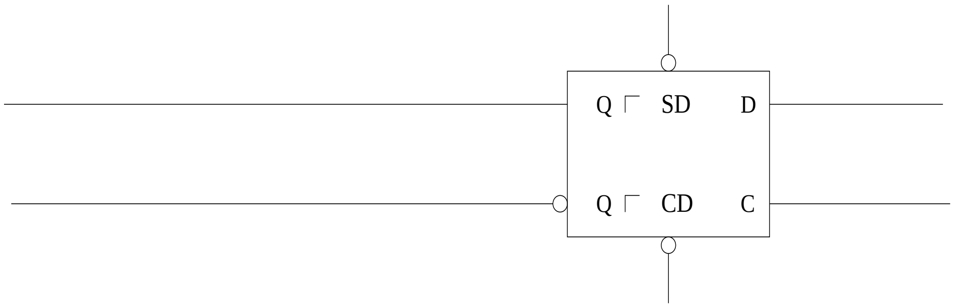
State	Encoding
`HG`	00
`HY`	01
`FG`	11
`FY`	10

Design your synchronous circuit as a Moore machine using two D flip flops (with asynchronous preset and clear). You must implement the next state combinational function using two 8 to 1 multiplexors. You must implement the output function using a maximum of four 2-input `nor` gates. The following incomplete logic schematic overviews the design you must employ.


I0
I1
I2
I3
I4
I5
I6
I7
Z
Z
S2
S1
S0
sto
lto
car


I0
I1
I2
I3
I4
I5
I6
I7
Z
Z
S2
S1
S0
sto
lto
car


Q
SD
D
Q
CD
C


Q
SD
D
Q
CD
C

Task: Develop the controller's state table.

Deliverable (D1): State table (using state names or state encoding).

Task: Design/develop the controller's combinational parts.

Deliverable (D2): Next state K-maps, D FF input K-maps and the output K-maps.

Task: Implement the next state and output functions using `nor` gates and multiplexors (as described previously).

Deliverable (D3): A completed logic schematic. All inputs and outputs must be shown.

Task: Develop a structural VHDL model of the sequential machine using the VHDL models for the TTL ICs SN74151, SN7474 and SN7402. You are allowed two instances of SN74151 and, one instance of each of the other two ICs. VHDL models can be found in `~csci355/Lab9`.

Deliverable (D3): Electronic submission of source code (`make submit`).

Task: Map your VHDL model to a TTL-based physical design for the sequential system.

Deliverable (D4): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D5): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D6): A physical realization of the sequential system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D7): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES