Experiment 6

Task (T1): Design a negative master-slave SR flip flop using `nor` gates and `and` gates.

Deliverable (D1): Logic schematic.

Task (T2): Design a TTL-based physical design for the negative master-slave SR flip flop.

Deliverable (D2): IC logic schematic.

Task (T3): Specify IC interconnections.

Deliverable (D3): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task (T4): In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D4): A physical realization of a negative master-slave SR flip flop that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Note In addition to demonstrating the *normal* behaviour of your circuit to the instructor, you must also demonstrate the phenomenon of ones catching using the test-case developed in conjunction with deliverable D1.

Task (T5): Document any relevant results, explanations or comments.

Deliverable (D5): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES