MALASPINA UNIVERSITY-COLLEGE
FINAL EXAMINATION DECEMBER 1999
COMPUTING SCIENCE CSCI 355

Instructor: Dr. P Walsh (F9901) **Duration:** 3 Hours.

TOTAL VALUE	100					
QUESTION	1	2	3	4	5	6
VALUE	10	10	10	25	25	20

Instructions

- Students must count the number of pages in this examination paper before beginning to write, and report any discrepancy immediately to the invigilator.
- This examination paper consists of 5 pages not including this cover page.
- Answer all questions in an answer booklet. All questions relate to material covered in class or in the lab. Show all your work.
- This is a CLOSED BOOK - examination. Students may consult notes written on one 8in. by 11 in. sheet of paper as described in class.
- Calculators are NOT permitted.

QUESTION 1.

Find a minimal sum of products expression for:

$$F(A, B, C, D, E) = \Sigma m(6, 7, 8, 9, 12, 13, 18, 22, 23, 24, 25, 28, 29)$$

QUESTION 2.

An NK latch has two inputs N and K and two outputs Q and Q_BAR. Input K behaves like the K input to a JK latch. Input N behaves like the complement of the J input to a JK latch.
Consider the following component declaration:

```
component NK is
   port (N: in bit; K: in bit; C: in bit;
         w: out bit; x: out bit; y: out bit; z: out bit);
end component;
```

The modeled device is a zero-delay NK single-bit memory comprising an NK latch, an NK gated latch with an active-high enable `C`, a negative master-slave NK flip flop with a clock `C` and a positive edge-triggered NK flip flop with a clock `C`. There are four outputs, one for each of the modeled NK latches/flip flops.

Your task is to develop test cases that can discriminate between the four NK latches/flip flops. You must explain your testing strategy in the form of annotated timing diagrams. If it is not possible to discriminate between some or all of the outputs then explain why.

QUESTION 3.

(a) Consider the following state table. It has one input X and out output Z. Your task is to identify any equivalent states.

Present State	Next State		Output	
	$X=0$	$X=1$	$X=0$	$X=1$
a	c	f	0	0
b	d	e	0	0
c	h	g	0	0
d	b	g	0	0
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1
h	c	f	0	0

QUESTION 4.

Consider the situation where you are given two D flip flops and two 8 to 1 multiplexors. The D flip flops are clocked edge-triggered devices with **no** asynchronous preset or clear. Your task is to design a 2-bit register using only the above devices. The register is to have three control lines $S0$, $S1$ and $S2$, two data-inputs x and y and two outputs $Z0$ and $Z1$. The register must support the following operations.

$S0$ $S1$ $S2$	Action
000	No change
001	circular shift left the register data
010	load the most significant register bit with x
011	load the least significant register bit with y
100	parallel load the register with x and y
101	complement the register data
110	clear the register data to all 0s
111	set the register data to all 1s

The register must behave as specified in the following state table.

Present State QA QB	Next State $S0$ $S1$ $S2$								Output $Z0$ $Z1$
	000	001	010	011	100	101	110	111	
00	00	00	x 0	0 y	x y	11	00	11	00
01	00	10	x 1	0 y	x y	10	00	11	01
10	00	01	x 0	1 y	x y	01	00	11	10
11	00	11	x 1	1 y	x y	00	00	11	11

Draw your design's logic schematic.

QUESTION 5.

Design a 2-bit counter that counts in the cyclic Grey codes

$$00_2\ 01_2\ 11_2\ 10_2\ 00_2\ 01_2\ \ldots$$

The counter accepts two synchronous control signals x and y and its behaviour is described in the following table. Note, let Z represent the present state and Z+1 the next state counting up in 2-bit cyclic Grey codes and Z-1 the previous state counting down in 2-bit cyclic Grey codes.

x	y	Next State	Action
0	0	Z+1	Up count
0	1	00	Clear count
1	0	11	Set count
1	1	Z-1	Down count

Design your synchronous circuit as a Moore machine using positive edge triggered NK[1] flip flops (with asynchronous preset and clear). Develop next state K-maps, NK flip flop input K-maps and output K-maps.

QUESTION 6.

Design a controller for a traffic light at the intersection of a highway and a farm-road. The behaviour of the controller is as follows. The highway lights remain green as long as there are no cars on the farm-road. When the highway lights have been green for a minimum of ten seconds, a car on the farm-road will cause the highway lights to go yellow for three seconds and then red. Then the farm-road lights will turn green and remain green for a minimum of three seconds. The presence of other cars on the farm-road beyond the three seconds will enable the farm-road lights to remain green for a maximum of ten seconds. The farm-road lights will then go yellow for three seconds and then red.

The controller is to have four states, highway green (`HG`), highway yellow (`HY`), farm-road green (`FG`) and farm-road yellow (`FG`). In state `HG`, the highway lights are green and the farm-road lights are red. In state `HY`, the highway lights are yellow and the farm-road lights are red. In state `FG`, the farm-road lights are green and the highway lights are red. In state `FY`, the farm-road lights are yellow and the highway lights are red. The controller is to have five control signals: `clear_BAR`, `car` , `sto`, `lto` and `clk`. The control signal `clear_BAR` is asynchronous. All other control signals are synchronous. When `clear_BAR` is asserted, the controller resets to state `HG`. When `car` is asserted, a car is present on the farm-road. When `lto` is asserted, a long-delay timer has reached the ten second mark. When `sto` is asserted, a short-delay timer has reached the three second mark.

There are five single-bit inputs and six single-bit outputs. The five inputs correspond to the control signals described earlier. Three of the outputs correspond to the red, green and yellow lights visible from the highway. They are `hw_R, hw_G, hw_Y`. The other three correspond to the red, green and yellow lights visible from the farm-road. They are `fr_R, fr_G, fr_Y`.

State transitions are shown in the following state diagram.

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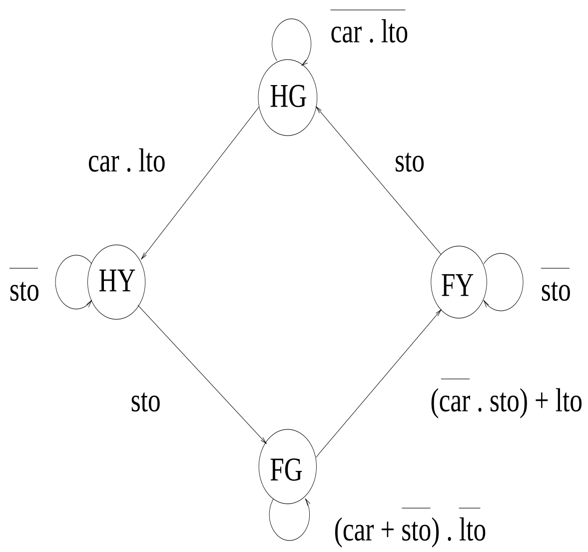
[1] An NK flip flop has two inputs N and K and two outputs Q and Q_BAR. Input K behaves like the K input to a JK flip flop. Input N behaves like the complement of the J input to a JK flip flop.



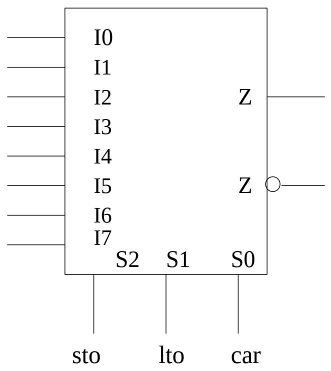
State assignment is shown in the following state assignment table.

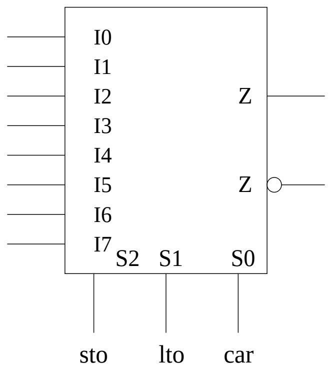
State	Encoding
`HG`	00
`HY`	01
`FG`	11
`FY`	10

Design your synchronous circuit as a Mealy machine using two D flip flops (with asynchronous preset and clear). You must implement the next state combinational function using two 8 to 1 multiplexors. You must implement the output function using a maximum of four 2-input `nor` gates. The following (last page of the exam paper)is an incomplete logic schematic that overviews the design you MUST employ.

Your task is to develop the controller's state table (using state names or state encoding). In addition, develop next state K-maps, D flip flop input K-maps and the output K-maps. You must implement the next state and output functions using `nor` gates and multiplexors (as described previously). Show the resulting design by completing the given logic schematic. NOTE, all inputs and outputs must be shown. Remove the completed logic schematic from the exam paper and include it in your answer booklet. **Make sure you put your name on the schematic.**

NAME ____________________________________


I0
I1
I2
I3
I4
I5
I6
I7
Z
Z
S2
S1
S0
sto
lto
car


I0
I1
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I3
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I5
I6
I7
Z
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S2
S1
S0
sto
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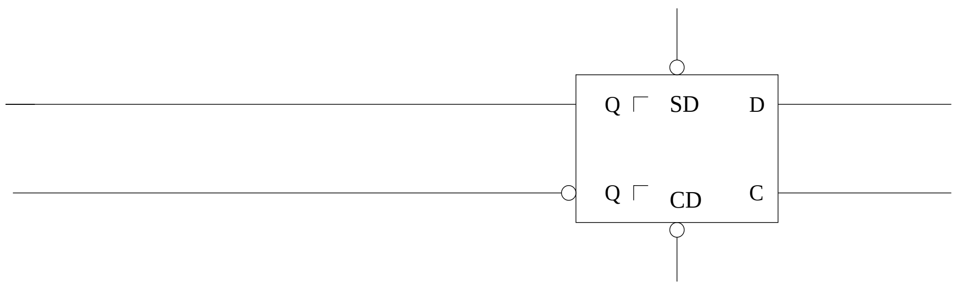
Q
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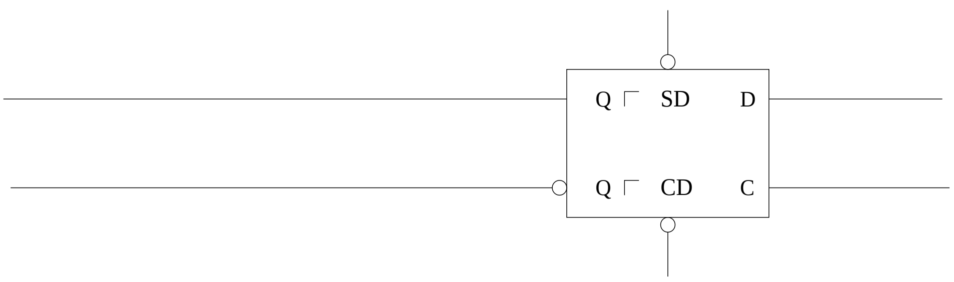
D
Q
CD
C


Q
SD
D
Q
CD
C