MALASPINA UNIVERSITY-COLLEGE
FINAL EXAMINATION DECEMBER 2003
COMPUTING SCIENCE CSCI 355

Instructor: Dr. P Walsh **Duration:** 3 Hours.

TOTAL VALUE	100					
QUESTION	1	2	3	4	5	6
VALUE	5	20	20	20	20	15

Instructions

- Students must count the number of pages in this examination paper before beginning to write, and report any discrepancy immediately to the invigilator.
- This examination paper consists of 3 pages not including this cover page.
- Answer all questions in an answer booklet. All questions relate to material covered in class or in the lab. Show all your work.
- This is a CLOSED BOOK - examination. Students may consult notes written on one 8in. by 11 in. sheet of paper as described in class.
- Calculators are NOT permitted.

QUESTION 1.

Find a minimal sum of products expression for:

$$F(A,B,C,D,E) = \Sigma m(8,12,13,14,15,22,28,29,30,31)$$

QUESTION 2.

An NK latch has two inputs N and K and two outputs Q and Q_BAR. Input K behaves like the K input to a JK latch. Input N behaves like the complement of the J input to a JK latch.
Consider the following component declaration:

```
component NK is
   port (N: in bit; K: in bit; C: in bit;
         w: out bit; x: out bit; y: out bit; z: out bit);
end component;
```

The modeled device is a zero-delay NK single-bit memory comprising an NK latch, an NK gated latch with an active-high enable `C`, a negative master-slave NK flip flop with a clock `C` and a positive edge-triggered NK flip flop with a clock `C`. There are four outputs, one for each of the modeled NK latches/flip flops.

Your task is to develop test cases that can discriminate between the four NK latches/flip flops. You must explain your testing strategy in the form of annotated timing diagrams. If it is not possible to discriminate between some or all of the outputs then explain why.

QUESTION 3.

Consider the FSM specified by the following state table.

Present State $QA\ QB$	Next State Input=X		Output $Z0\ Z1$
	X=0	X=1	
00	01	10	01
01	01	11	11
10	11	00	10
11	00	11	11

(a) Obtain minimum excitation equation(s) for S-R flip-flops using K-map(s).
(b) Obtain excitation equation(s) for D flip-flops using inspection.
(c) Obtain minimum output equation(s) using K-map(s).

QUESTION 4.

Consider the FSM specified by the following state table.

Present State $QA\ QB\ QC\ QD$	Next State Input=X		Output $Z0\ Z1$	
	X=0	X=1	X=0	X=1
0001	1000	0010	00	01
0010	1000	0100	00	10
0100	0001	1000	00	00
1000	0100	0001	00	11

(a) Obtain minimum excitation equation(s) for T flip-flops using K-map(s).
(b) Obtain excitation equation(s) for J-K flip-flops using inspection.
(c) Obtain output equation(s) using inspection.

QUESTION 5.

Design a single-purpose processor that outputs *sigmaRX(n)* where

$$n \geq 0$$

$$sigmaRX(0) = 0$$

$$sigmaRX(1) = 1$$

$$sigmaRX(n) = n + sigmaRX(n-2)$$

For example, $sigmaRX$(7)=7+5+3+1=16 and $sigmaRX$(8)=8+6+4+2+0=20.

Start off with an iterative function computing the desired result. Then derive the datapath and control unit. Note, all registers are to be 8 bits wide.

QUESTION 6.

(a) Consider the following state table. It has one input X and out output Z. Your task is to identify any equivalent states.

Present State	Next State $X=0$	Next State $X=1$	Output Z
a	b	c	1
b	d	f	1
c	f	e	0
d	b	g	1
e	f	c	1
f	e	d	1
g	f	g	1

(b) With regard to the FSM specified in QUESTION 3, implement the FSM using a 2-bit counter. The counter has a 2-bit input `I`, a 2-bit output `O` and the control lines `clear,` `count` and `load`. `clear` clears the counter to zero, `count` increments the value of the counter by 1 modulo 4 and `load` parallel loads the counter with `I`.

The control lines have no priority.

You must clearly indicate how you derived the combinational components that drive next-state transitions and outputs.

Draw a logic schematic of your design.