MALASPINA UNIVERSITY-COLLEGE
FINAL EXAMINATION DECEMBER 2002
COMPUTING SCIENCE CSCI 355

Instructor: Dr. P Walsh (F0001) **Duration:** 3 Hours.

TOTAL VALUE	100					
QUESTION	1	2	3	4	5	6
VALUE	10	20	20	20	15	15

Instructions

- Students must count the number of pages in this examination paper before beginning to write, and report any discrepancy immediately to the invigilator.
- This examination paper consists of 3 pages not including this cover page and 1 VHDL handout.
- Answer all questions in an answer booklet. All questions relate to material covered in class or in the lab. Show all your work.
- This is a CLOSED BOOK - examination. Students may consult notes written on one 8in. by 11 in. sheet of paper as described in class.
- Calculators are NOT permitted.

QUESTION 1.

Find a minimal product of sums expression for:

$$F(A,B,C,D,E) = \Pi\ M(6,7,8,9,12,13,18,22,23,24,25,28,29)$$

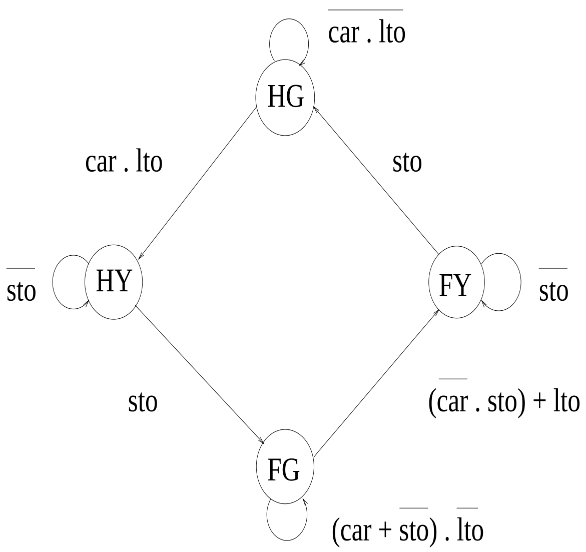
QUESTION 2.

Design a controller for a traffic light at the intersection of a highway and a farm-road. The behaviour of the controller is as follows. The highway lights remain green as long as there are no cars on the farm-road. When the highway lights have been green for a minimum of ten seconds, a car on the farm-road will cause the highway lights to go yellow for three seconds and then red. Then the farm-road lights will turn green and remain green for a minimum of three seconds. The presence of other cars on the farm-road beyond the three seconds will enable the farm-road lights to remain green for a maximum of ten seconds. The farm-road lights will then go yellow for three seconds and then red.

The controller is to have four states, highway green (`HG`), highway yellow (`HY`), farm-road green (`FG`) and farm-road yellow (`FY`). In state `HG`, the highway lights are green and the farm-road lights are red. In state `HY`, the highway lights are yellow and the farm-road lights are red. In state `FG`, the farm-road lights are green and the highway lights are red. In state `FY`, the farm-road lights are yellow and the highway lights are red. The controller is to have five control signals: `clear_BAR`, `car` , `sto`, `lto` and `clk`. The control signal `clear_BAR` is asynchronous. All other control signals are synchronous. When `clear_BAR` is asserted, the controller resets to state `HG`. When `car` is asserted, a car is present on the farm-road. When `lto` is asserted, a long-delay timer has reached the ten second mark. When `sto` is asserted, a short-delay timer has reached the three second mark.

There are five single-bit inputs and six single-bit outputs. The five inputs correspond to the control signals described earlier. Three of the outputs correspond to the red, green and yellow lights visible from the highway. They are `hw_R, hw_G, hw_Y`. The other three correspond to the red, green and yellow lights visible from the farm-road. They are `fr_R, fr_G, fr_Y`.

State transitions are shown in the following state diagram.



State assignment is shown in the following state assignment table.

State	Encoding
HG	00
HY	01
FG	11
FY	10

Design your synchronous circuit as a Mealy machine using a 2-bit counter. The counter has a 2-bit input `I`, a 2-bit output `O` and the control lines `clear,` `count` and `load`. `clear` clears the counter to zero, `count` increments the value of the counter by 1 modulo 4 and `load` parallel loads the counter with `I`. The control lines have no priority.

You must clearly indicate how you derived the combinational components that drive next-state transitions and outputs.

Draw a logic schematic of you design.

QUESTION 3.

Design a 2-bit counter that counts in the cyclic Grey codes

$$00_2\ 01_2\ 11_2\ 10_2\ 00_2\ 01_2\ \ldots$$

The counter accepts two synchronous control signals x and y and its behaviour is described in the following table. Note, let Z represent the present state and $Z{+}1$ the next state counting up in 2-bit cyclic Grey codes.

x	y	Next State	Action
0	0	Z+1	Up count
0	1	00	Clear count
1	0	11	Set count
1	1	-	Illegal input

Design your synchronous circuit as a Moore machine using positive edge triggered JK flip flops (with asynchronous preset and clear). Develop next state K-maps, JK flip flop input K-maps and output K-maps.

QUESTION 4.

Consider a Mealy synchronous machine consisting of 3 D flip flops and some combinational logic. The machine has one input X and one output Z. The flip flop input equations and the output equation are

$$D_A = (Q_A \cdot \overline{Q_C} \cdot \overline{X})$$

$$D_B = (\overline{Q_A} \cdot X)$$

$$D_C = (\overline{Q_C} \cdot \overline{X}) + (\overline{Q_A} \cdot \overline{Q_B} \cdot Q_C) + (\overline{Q_B} \cdot Q_C \cdot \overline{X})$$

$$Z = (Q_A \cdot X) + (Q_B \cdot Q_C \cdot \overline{X})$$

Draw the circuit diagram that corresponds to the above machine and tabulate its next state and output in a state table.

Identify any equivalent states.

QUESTION 5.

Compare and contrast a register file and a RAM.

Design a 3 x 2 (3 registers, each register is 2 bits wide) with two write and two read ports using decoders and RFCs.

QUESTION 6.

Consider the ram6116 component detailed in the `ram6116.vhd` handout. It is a model of a 256 x 8 static RAM (256 words, each word is 8 bits wide).

Using the ram6116 and some combinational components, design a 256 x 16 memory system and a 1K x 8 memory system.

In both cases, you must detail your design by drawing a logic schematic and you must clearly label data and address busses.