MALASPINA UNIVERSITY-COLLEGE
FINAL EXAMINATION DECEMBER 2000
COMPUTING SCIENCE CSCI 355

Instructor: Dr. P Walsh (F0001) **Duration:** 3 Hours.

TOTAL VALUE	100					
QUESTION	1	2	3	4	5	6
VALUE	10	20	20	15	15	20

Instructions

- Students must count the number of pages in this examination paper before beginning to write, and report any discrepancy immediately to the invigilator.
- This examination paper consists of 4 pages not including this cover page and 8 pages of VHDL code.
- Answer all questions in an answer booklet. All questions relate to material covered in class or in the lab. Show all your work.
- This is a CLOSED BOOK - examination. Students may consult notes written on one 8in. by 11 in. sheet of paper as described in class.
- Calculators are NOT permitted.

QUESTION 1.

Find a minimal sum of products expression for:

$$F(A, B, C, D, E) = \Sigma m(6, 7, 8, 9, 12, 13, 18, 22, 23, 24, 25, 28, 29)$$

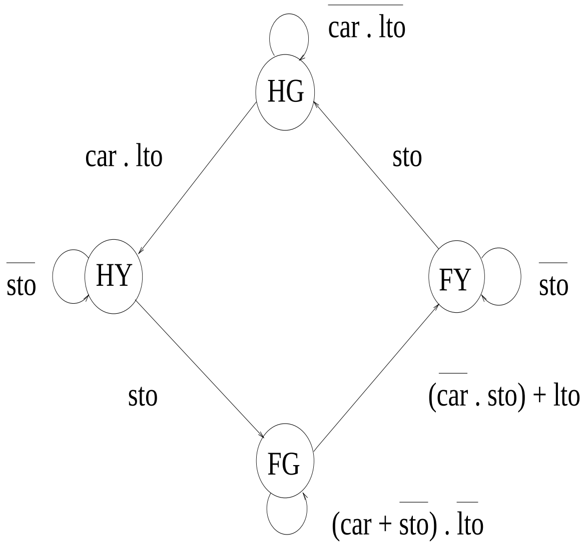
QUESTION 2.

Design a controller for a traffic light at the intersection of a highway and a farm-road. The behaviour of the controller is as follows. The highway lights remain green as long as there are no cars on the farm-road. When the highway lights have been green for a minimum of ten seconds, a car on the farm-road will cause the highway lights to go yellow for three seconds and then red. Then the farm-road lights will turn green and remain green for a minimum of three seconds. The presence of other cars on the farm-road beyond the three seconds will enable the farm-road lights to remain green for a maximum of ten seconds. The farm-road lights will then go yellow for three seconds and then red.

The controller is to have four states, highway green (`HG`), highway yellow (`HY`), farm-road green (`FG`) and farm-road yellow (`FG`). In state `HG`, the highway lights are green and the farm-road lights are red. In state `HY`, the highway lights are yellow and the farm-road lights are red. In state `FG`, the farm-road lights are green and the highway lights are red. In state `FY`, the farm-road lights are yellow and the highway lights are red. The controller is to have five control signals: `clear_BAR`, `car` , `sto`, `lto` and `clk`. The control signal `clear_BAR` is asynchronous. All other control signals are synchronous. When `clear_BAR` is asserted, the controller resets to state `HG`. When `car` is asserted, a car is present on the farm-road. When `lto` is asserted, a long-delay timer has reached the ten second mark. When `sto` is asserted, a short-delay timer has reached the three second mark.

There are five single-bit inputs and six single-bit outputs. The five inputs correspond to the control signals described earlier. Three of the outputs correspond to the red, green and yellow lights visible from the highway. They are `hw_R, hw_G, hw_Y`. The other three correspond to the red, green and yellow lights visible from the farm-road. They are `fr_R, fr_G, fr_Y`.

State transitions are shown in the following state diagram.



One-hot state assignment is shown in the following state assignment table.

State	Encoding
HG	0001
HY	0010
FG	0100
FY	1000

Design your synchronous circuit as a Mealy machine using four D flip flops (with asynchronous preset and clear). To this end, develop the controller's state table (using state names or state encoding). In addition, develop next state K-maps, D flip flop input K-maps and the output K-maps.

QUESTION 3.

Consider the following state table (with state encodings). It has one input X and six states. Your task is implement this system using a modulo 16 parallel-load up counter, a 8 to 1 multiplexor and 4 inverters.

Present State	Next State	
	X=0	X=1
000	001	001
001	010	010
010	101	011
011	100	100
100	011	011
101	010	010

Questions 4, 5 and 6 refer to second part of the third assignment (stack machine). VHDL code is given at the end of this exam paper.

QUESTION 4.

Draw a state diagram that details state transitions for the load-phase of the stack machine specified in the VHDL code at the end of the exam paper. Develop the load-phase state table (using state names or state encoding), next state K-maps and D flip flop input K maps.

State	Encoding
`Idle`	000
`L1`	001
`L2`	010
`L3`	011
`L4`	100

QUESTION 5.

The load phase of the stack machine is concerned with the following inputs `initPC, incPC, loadMem, x`. Your task is to design the data path at the structural level using a memory component with separate data in, data out and address busses and, a parallel load up counter for the program counter. To keep things simple, your design need not consider the execution phase and clock signals are not shown. Detail your design by completing the following logic schematic.

QUESTION 6.

The `swap` instruction takes two 4 bit argument in the following form:
`swap low4bits  high4bits`. The `swap` instruction swaps the contents of the word referenced by the SP with the word referenced by the address formed by the concatenation of `high4bits` and `low4bits`.

Your task is to add the `swap` instruction to the stack machine. Augment the given code to support the new instruction. You are allowed one additional index register in the data path called `SI`. The new register is 8 bits wide. Your are free to determine its use in the data path and augment the data path interface in the appropriate way.

Restrictions: Only one memory read can occur in a clock cycle. Only one memory write can occur in a clock cycle.