MALASPINA UNIVERSITY-COLLEGE
FINAL EXAMINATION DECEMBER 1998
COMPUTING SCIENCE CSCI 355

Instructor: Dr. P Walsh **Duration:** 3 Hours.

TOTAL VALUE	100							
QUESTION	1	2	3	4	5	6	7	8
VALUE	5	5	15	10	20	10	20	15

Instructions

- Students must count the number of pages in this examination paper before beginning to write, and report any discrepancy immediately to the invigilator.
- This examination paper consists of 4 pages not including this cover page.
- Answer all questions in an answer booklet. All questions relate to material covered in class or in the lab. Show all your work.
- This is a CLOSED BOOK - examination. Students may consult notes written on one 8in. by 11 in. sheet of paper as described in class.
- Calculators are NOT permitted.

QUESTION 1.

Find a minimal sum of products expression for:

$$F(A,B,C,D,E) = \Sigma m(0,2,4,6,9,13,21,23,25,29,31)$$

QUESTION 2.

Develop a structural description of COMPARE using only 4 2-input NOR gates. Draw the circuit diagram ONLY (ie, you are not being asked to give any VHDL code).

```
entity COMPARE is
port (a,b: in bit;
      c: out bit);
end COMPARE;

architecture dataflow COMPARE is
      begin
      c <= NOT (a XOR b);
end dataflow;
```

QUESTION 3.

Consider the following function.

$$F(A,B,C,D) = \Sigma m(0,2,3,4,9,11,12,13,14)$$

(a) Implement the F using an 8-to-1 multiplexor. You must assign the variables A, B and C to the control lines (in order) and you may assume that the true and complemented form of variable D is available.

(b) Implement F using a 4-line to 16-line decoder with inverted outputs (ie., outputs are asserted low) and some extra combinational logic.

QUESTION 4.

An NK latch has two inputs N and K and two outputs Q and Q_BAR. Input K behaves like the K input to a JK latch. Input N behaves like the complement of the J input to a JK latch.

(a) Derive the characteristic equation for the NK latch and tabulate its excitation table.

(b) Design a D latch using a NK latch and design a T latch using a NK latch and a NOR gate.

QUESTION 5.

Consider a Mealy synchronous machine consisting of 3 D flip flops and some combinational logic. The machine has one input X and one output Z. The flip flop input equations and the output equation are

$$D_A = (Q_A \cdot \overline{Q_C} \cdot \overline{X})$$

$$D_B = (\overline{Q_A} \cdot X)$$

$$D_C = (\overline{Q_C} \cdot \overline{X}) + (\overline{Q_A} \cdot \overline{Q_B} \cdot Q_C) + (\overline{Q_B} \cdot Q_C \cdot \overline{X})$$

$$Z = (Q_A \cdot X) + (Q_B \cdot Q_C \cdot \overline{X})$$

Your task is to draw the circuit diagram that corresponds to the above machine and tabulate its next state and output in a state table.

QUESTION 6.

(a) Consider the following state table. It has one input X and out output Z. Your task is to identify any equivalent states.

Present State	Next State		Output
	X=0	X=1	
a	e	c	0
b	h	d	0
c	d	g	0
d	h	e	1
e	f	d	1
f	b	e	0
g	e	a	0
h	f	d	0

(b) Consider the following state table. It has one input X and out output Z. Your task is to identify the sets of adjacent states as suggested by each of the Armstrong-Humphrey Rules.

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
a	b	c	0	0
b	b	d	0	0
c	e	c	0	0
d	a	c	1	0
e	b	a	0	1
f	a	a	0	0
g	a	a	0	0
h	a	a	0	0

QUESTION 7.

Design a 2-bit counter that counts in the cyclic Grey codes

$$00_2\ 01_2\ 11_2\ 10_2\ 00_2\ 01_2\ ...$$

The counter accepts two synchronous control signals to set and clear the count, as described below.

SET	CLR	Z^+	Action
0	0	Z+1	Up count
0	1	00	Clear count
1	0	11	Set count
1	1	-	Illegal input

Design your synchronous circuit as a Moore machine using positive edge triggered JK flip flops. Derive the minimized output and next state (memory device input) logic expressions. Draw the corresponding logic diagram.

QUESTION 8.

Consider the following concurrent signal assignment statements. Generate a timing diagram containing waveforms for the signals SYNC_BAR, A, B, W, X, Y and Z. The diagram should detail signal values from time=0 to time=40min. Assume that

- SYNC_BAR is initialized to '1' and changes to '0' after 20 minutes
- A, B, W, X, Y and Z are all initialized to '0'
- A changes to '1' after 5 minutes and returns to '0' 25 minutes later (at the 30 minute mark)

- B changes to '1' after 10 minutes and returns to '0' 3 minutes later (at the 13 minute mark)

```
B1: block (SYNC_BAR = '0')
begin
   W <= guarded A or B after 5 min;
   X <= A or B after 5 min;
   Y <='1' after 10 min, '0' after 20 min;
   Z <= guarded '1' after 5 min;
end block B1;
```