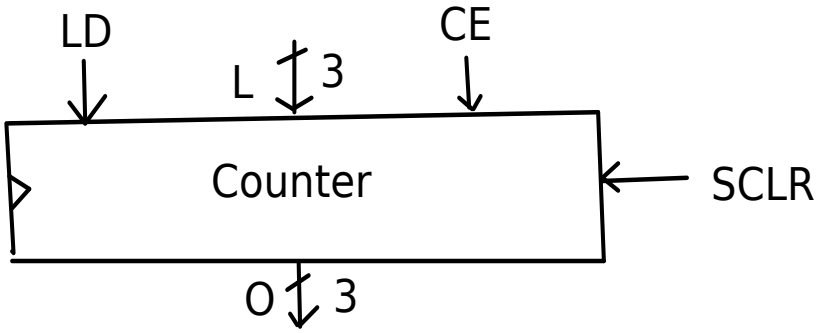
# Computer Science CSCI 355

# Digital Logic and Computer Organization

*Dr. Peter Walsh*
*Department of Computer Science*
*Vancouver Island University*
*peter.walsh@viu.ca*

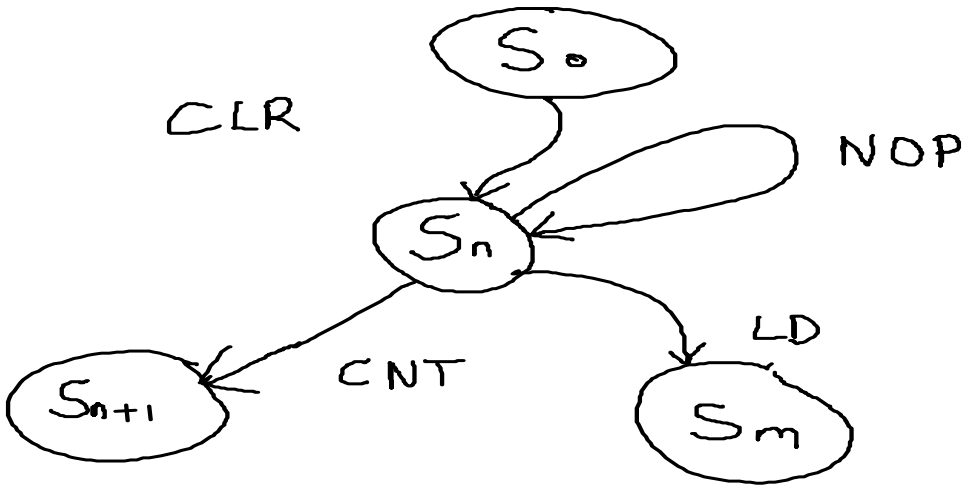
# Counters

| LD | CE | SCLR | L[2:0] | Operation | | Priority |
|---|---|---|---|---|---|---|
| 1 | - | - | value | load value | LD | 0 |
| 0 | 1 | 0 | - | count up | CNT | 1 |
| 0 | 0 | 1 | - | clear | CLR | 2 |
| 0 | 0 | 0 | - | nop | NOP | 3 |

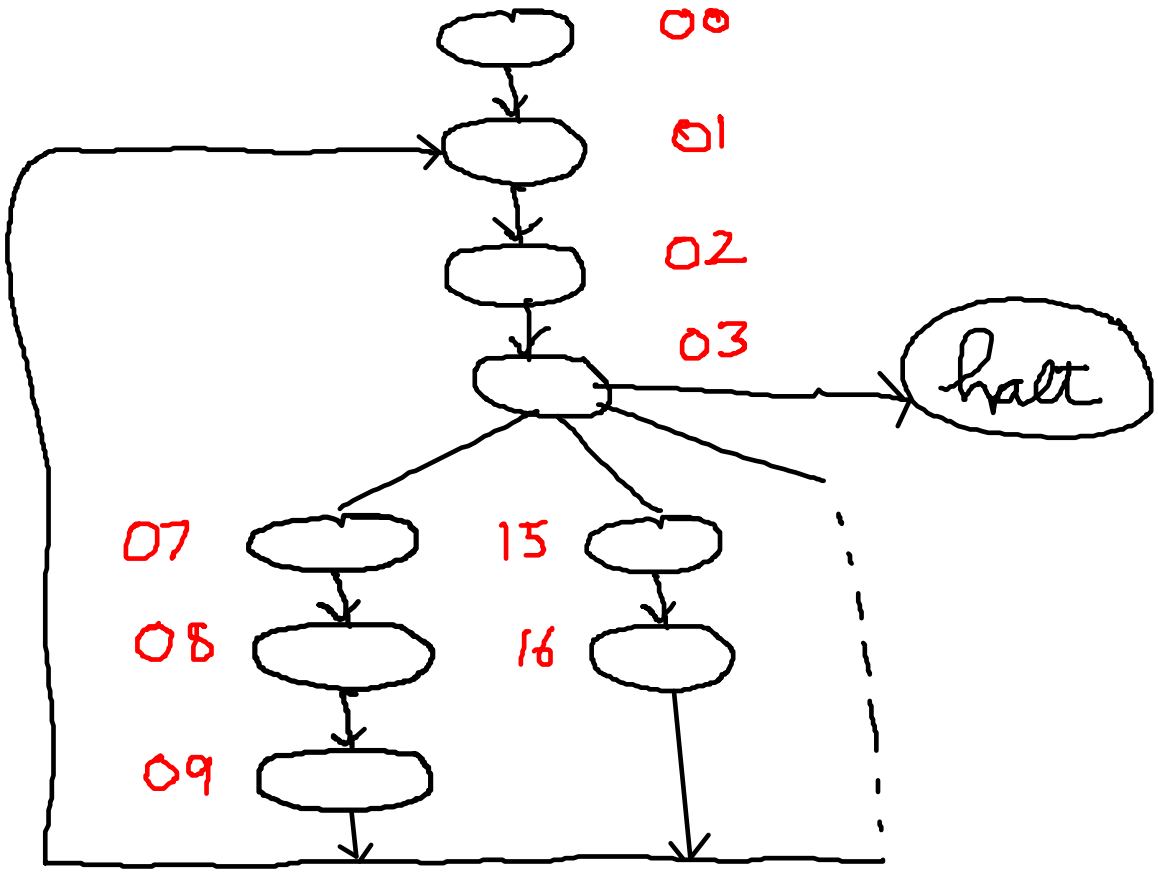


# FSMs Using Counters

- use the counter to store state

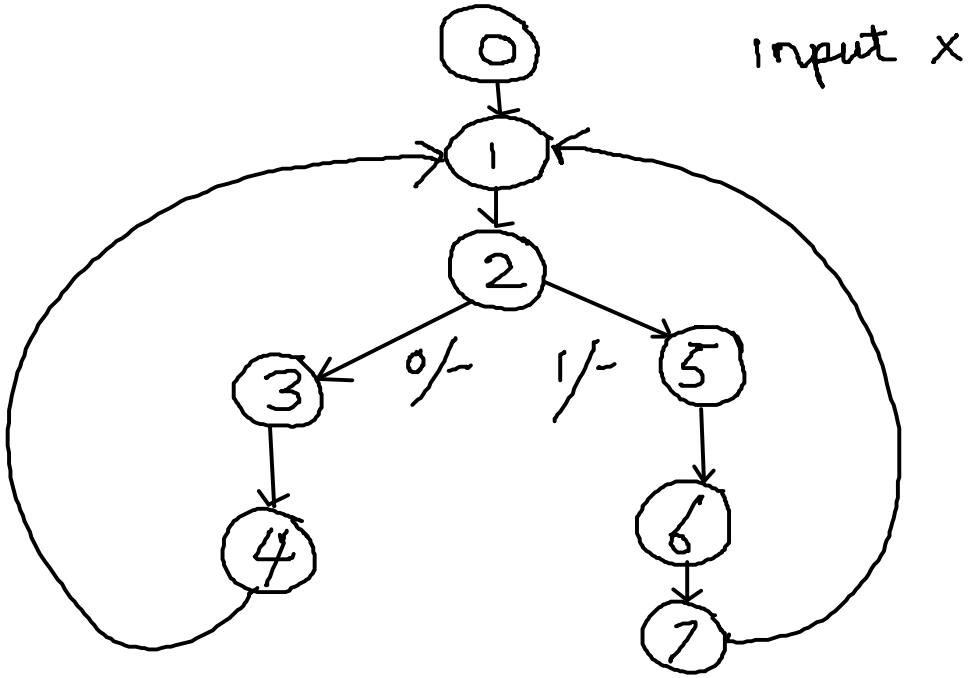


# SSBC Control Unit

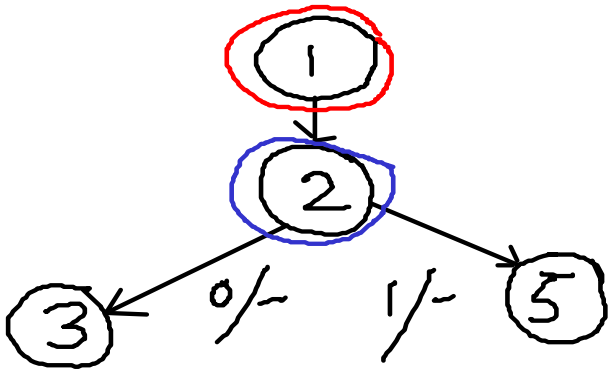


# FSM Implementation Example

- implement state transition using a 3-bit counter



# FSM Implementation Example cont.




Q

| Q2 | Q1 | Q0 | X | LD | CE | SCLR | L2 | L1 | L0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | - | - | - |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | - | - | - |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | - | - | - |
| 0 | 1 | 0 | 1 | 1 | - | - | 1 | 0 | 1 |

# FSM Implementation Example cont.

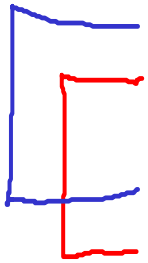
| Q2 | Q1 | Q0 | X | LD | CE | SCLR | L2 | L1 | L0 | State |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | - | - | - | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | - | - | - | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | - | - | - | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | - | - | - | |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | - | - | - | 2 |
| 0 | 1 | 0 | 1 | 1 | - | - | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | - | - | - | 3 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | - | - | - | |
| 1 | 0 | 0 | 0 | 1 | - | - | 0 | 0 | 1 | 4 |
| 1 | 0 | 0 | 1 | 1 | - | - | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | - | - | - | 5 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | - | - | - | |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | - | - | - | 6 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | - | - | - | |
| 1 | 1 | 1 | 0 | 1 | - | - | 0 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 1 | - | - | 0 | 0 | 1 | |

# State Minimization

- Equivalent States
  - two states are equivalent if they have the same next state and output
- Minimization Techniques
  - Row Comparison
  - Implication Table

# Row Comparison)

| Current State | Next State X=0 | Next State X=1 | Output |
|---|---|---|---|
| S0 | S1 | S0 | 0 |
| S1 | S2 | S0 | 0 |
| S2 | S3 | S6 | 0 |
| S3 | S0 | S4 | 0 |
| S4 | S5 | S0 | 0 |
| S5 | S0 | S0 | 1 |
| S6 | S7 | S0 | 0 |
| S7 | S8 | S0 | 0 |
| S8 | S0 | S0 | 1 |

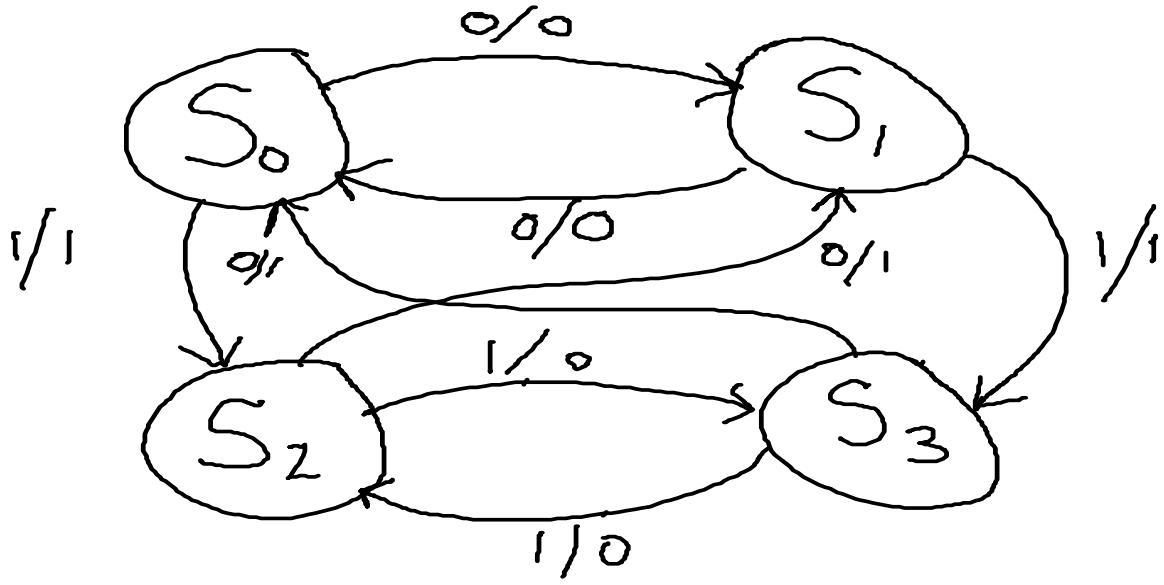


Replace S8 with S5

Replace S7 with S4

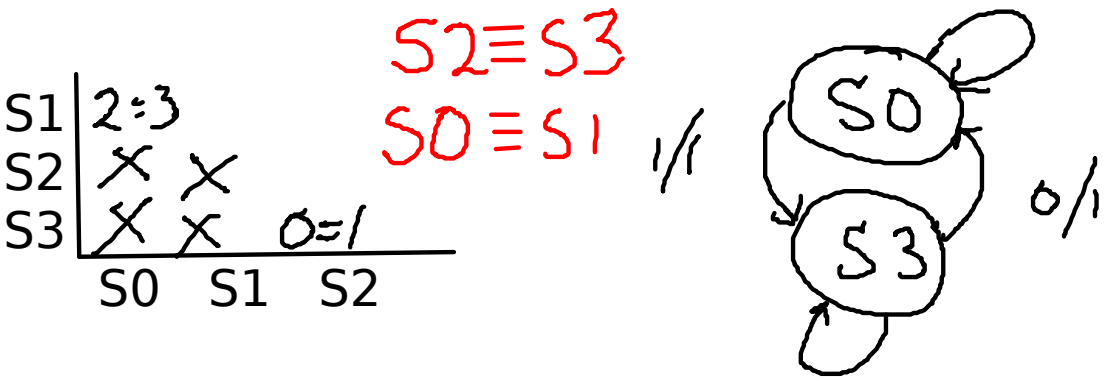
# Implication Table

- contrived example



# Implication Table cont.

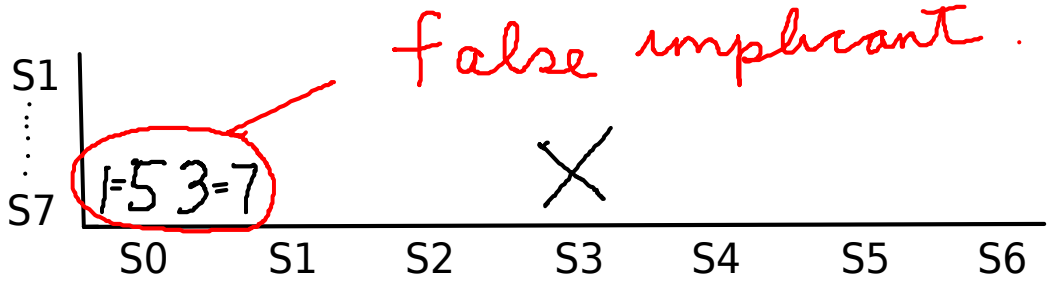
| Current State | Next State | | Output | |
|---|---|---|---|---|
| | X=0 | X=1 | X=0 | X=1 |
| S0 | S1 | S2 | 0 | 1 |
| S1 | S0 | S3 | 0 | 1 |
| S2 | S1 | S3 | 1 | 0 |
| S3 | S0 | S2 | 1 | 0 |



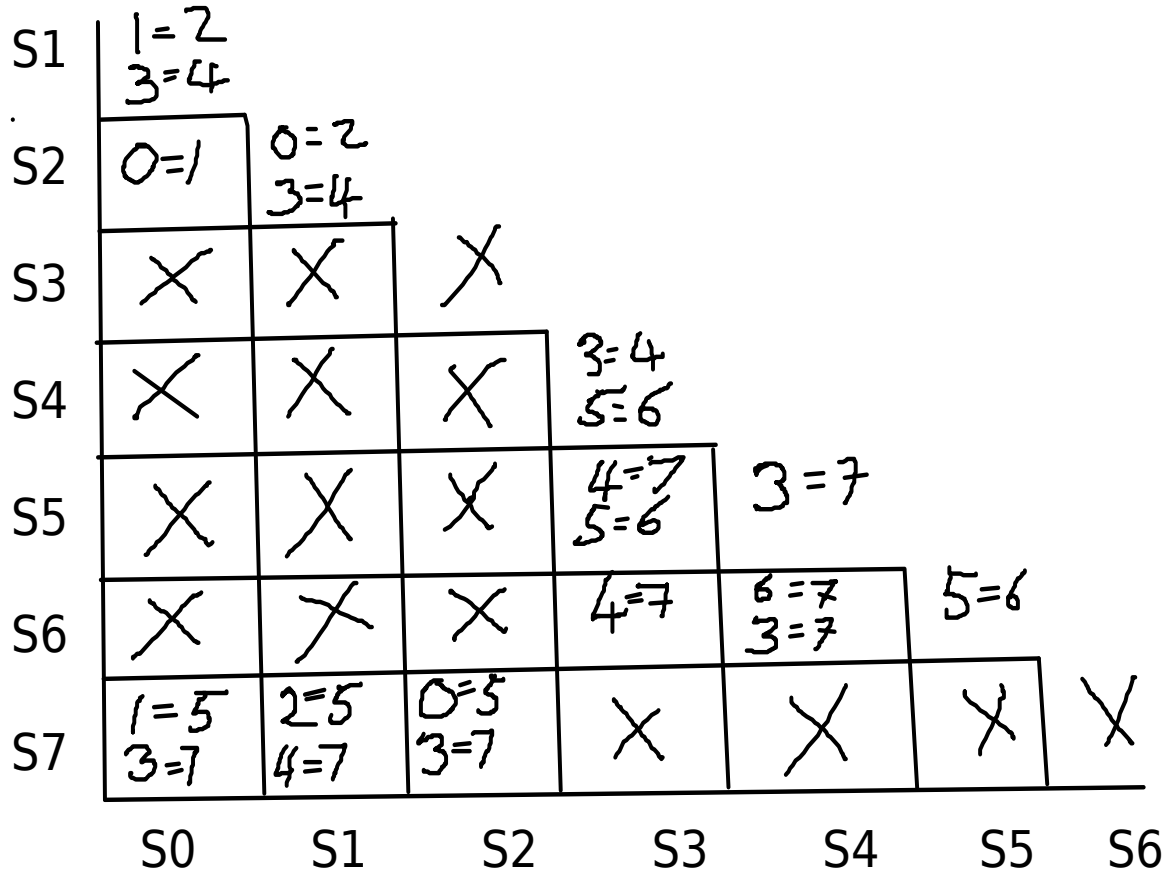
# Implication Table

- a second example

| Current State | Next State X=0 | Next State X=1 | Output |
|---|---|---|---|
| S0 | S1 | S3 | 0 |
| S1 | S2 | S4 | 0 |
| S2 | S0 | S3 | 0 |
| S3 | S4 | S5 | 1 |
| S4 | S3 | S6 | 1 |
| S5 | S7 | S6 | 1 |
| S6 | S7 | S5 | 1 |
| S7 | S5 | S7 | 0 |



# Implication Table cont.



# Implication Table cont.