

Computer Science CSCI 355

Digital Logic and Computer Organization

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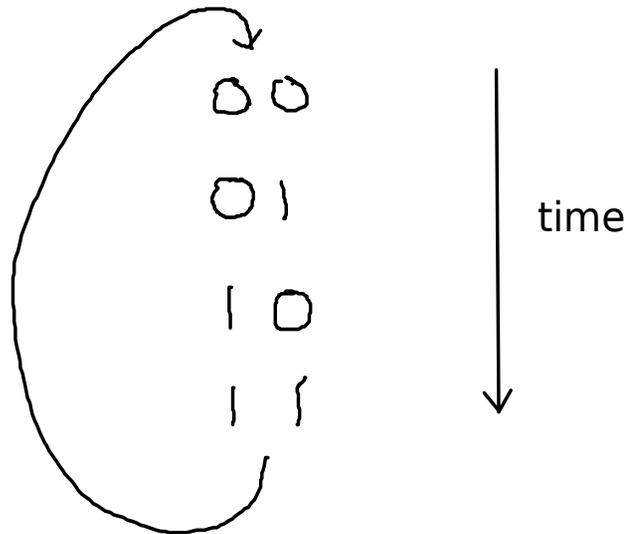
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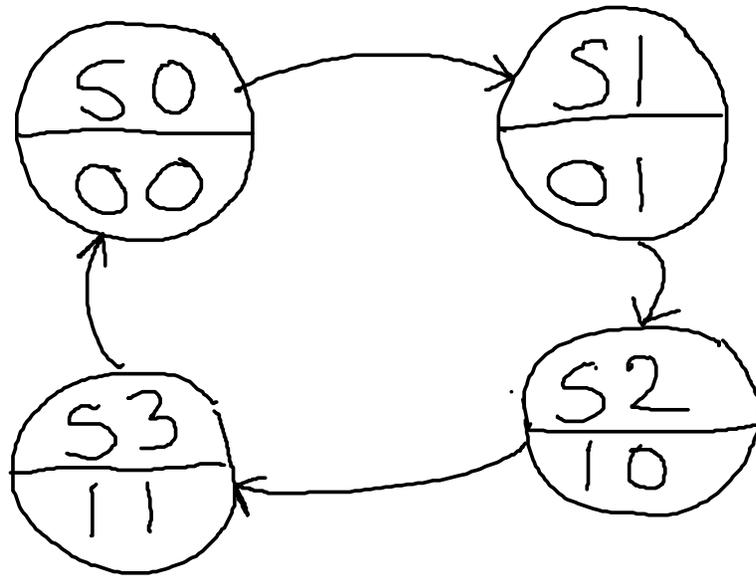
Ring Counter

Task: design and construct a two-bit ring counter using T edge triggered flip flops.



No inputs. Two outputs Z_1, Z_2 .

FSM (Step 5)



State Table (Step 4)

Present State	Next State	Output		Encoding	
Q	Q+	Z1	Z2		
S0	S1	0	0	0	0
S1	S2	0	1	0	1
S2	S3	1	0	1	0
S3	S0	1	1	1	1

State Table cont. (Step 4)

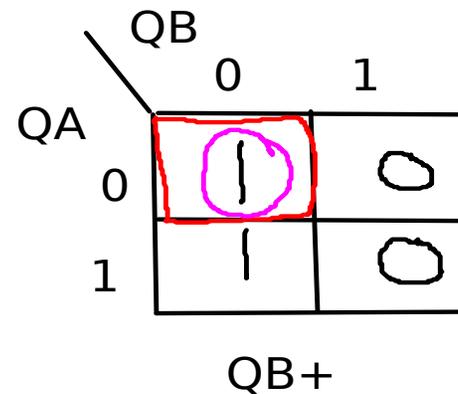
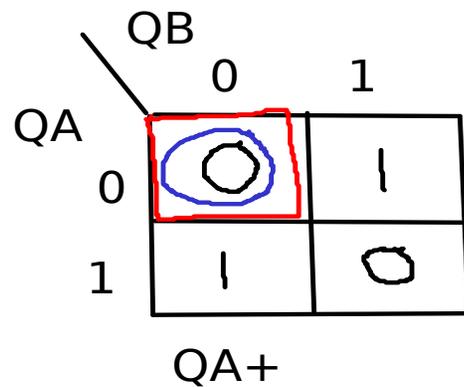
QA QB

Present State	Next State	Output
00	01	00
01	10	01
10	11	10
11	00	11

K Map Construction (Step 3)

QA QB

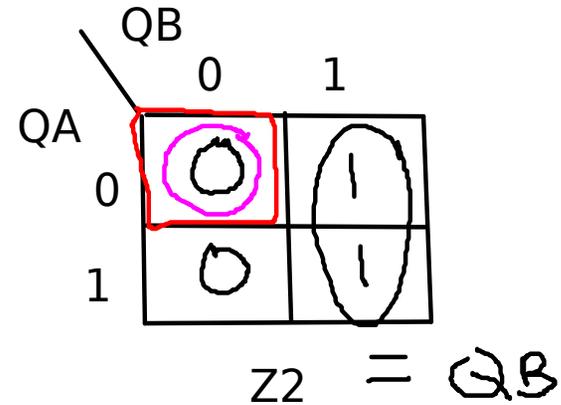
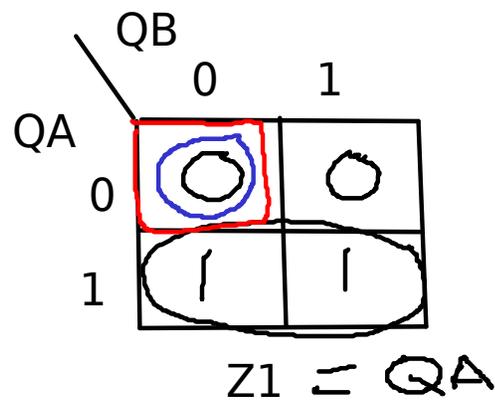
Present State	Next State	Output
00	→ 01 ←	00
01	10	01
10	11	10
11	00	11



K Map Construction cont. (Step 3)

QA QB

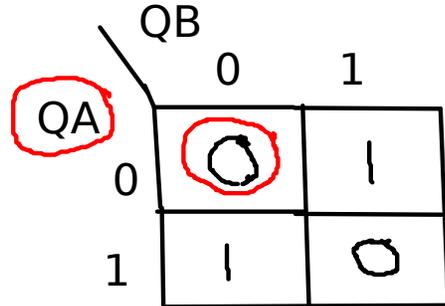
Present State	Next State	Output
00	01	00
01	10	01
10	11	10
11	00	11



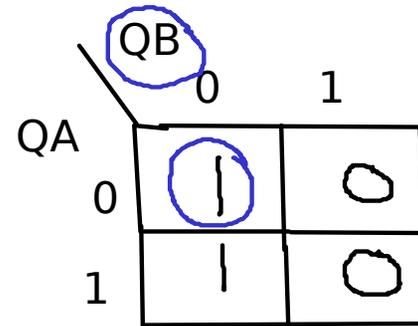
Excitation Tables

Q	Q+	S	R	J	K	T	D
0	0	0	-	0	-	0	0
0	1	1	0	1	-	1	1
1	0	0	1	-	1	1	0
1	1	-	0	-	0	0	1

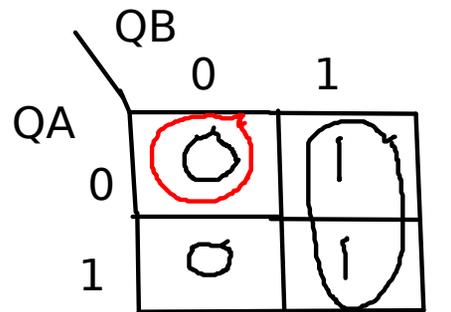
FF-Input Equations (Step 2)



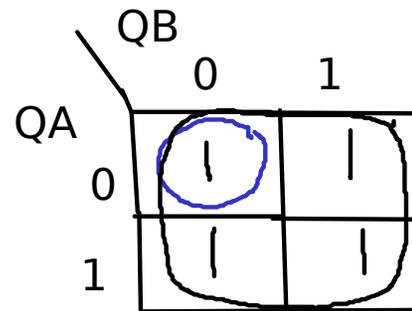
QA+



QB+



TA = QB



TB = 1

Circuit Diagram (Step 1)

$$Z1 = QA$$

$$\overline{TA} = QB$$

$$\overline{TB} = 1$$

$$Z2 = QB$$

