Computer Science CSCI 355

Digital Logic and Computer Organization

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Department of Computer Science
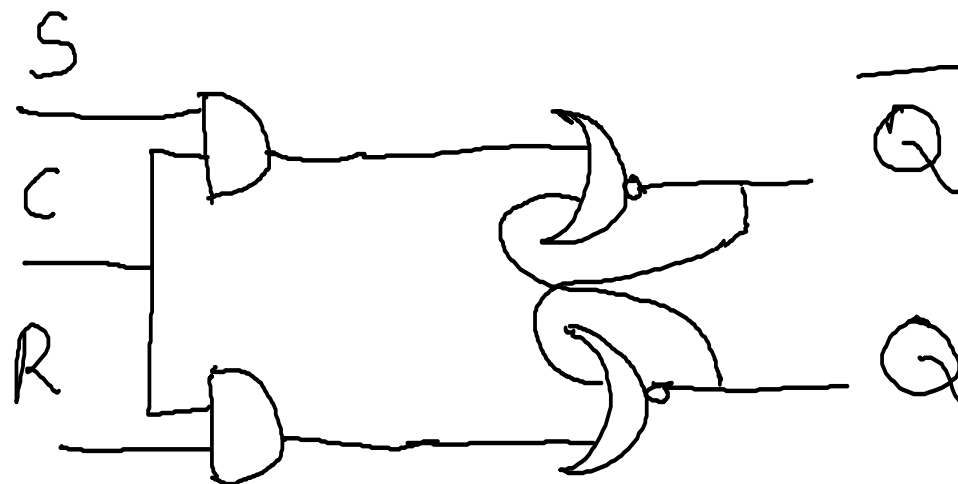
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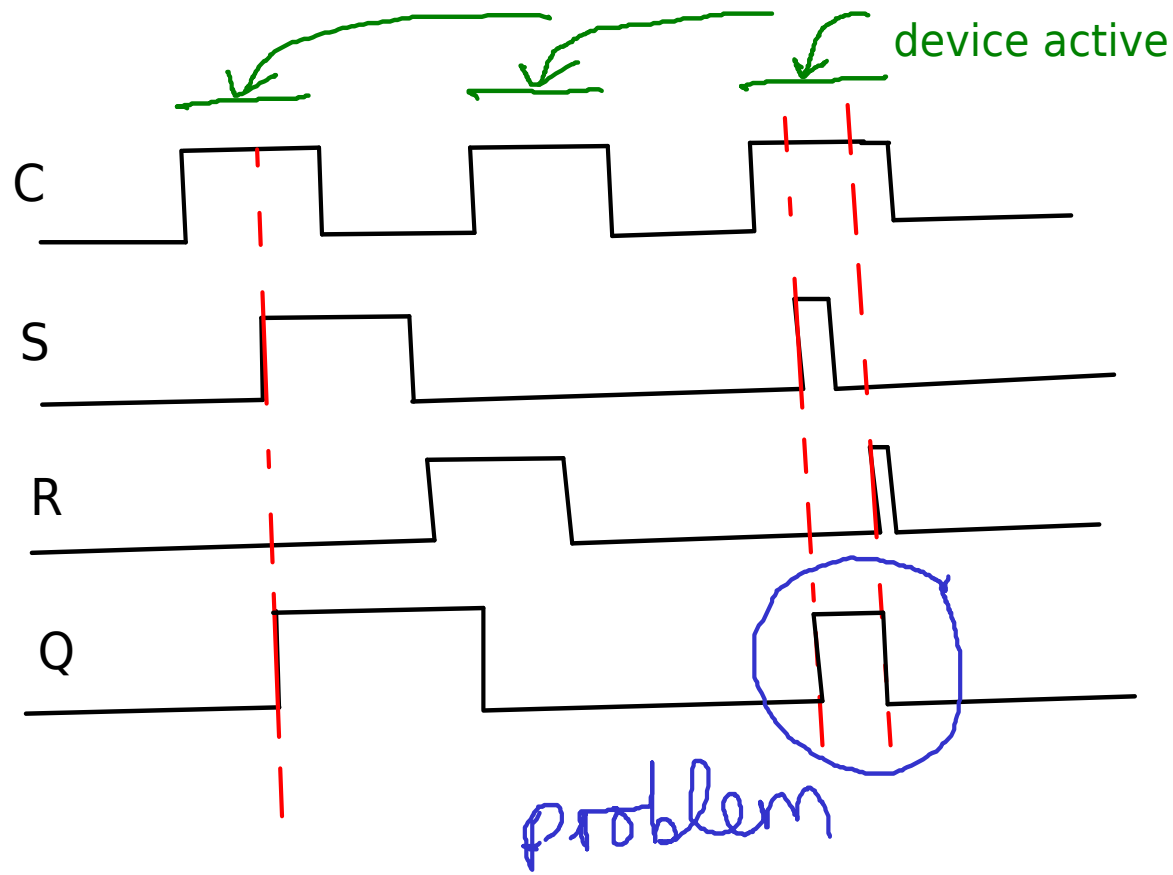# Synchronous Sequential Systems

Latches are not well suited for synchronous sequential systems because they operate in an asynchronous fashion.

○ Inputs Change
  - latch outputs are updated according
    to the appropriate characteristic equation
○ Result
  - erratic state changes
○ Fix
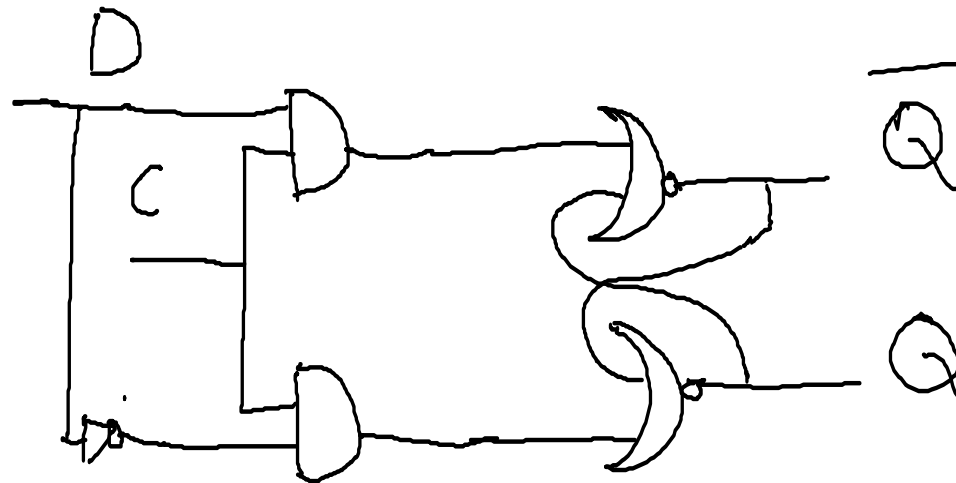 - impose a synchronous timing discipline
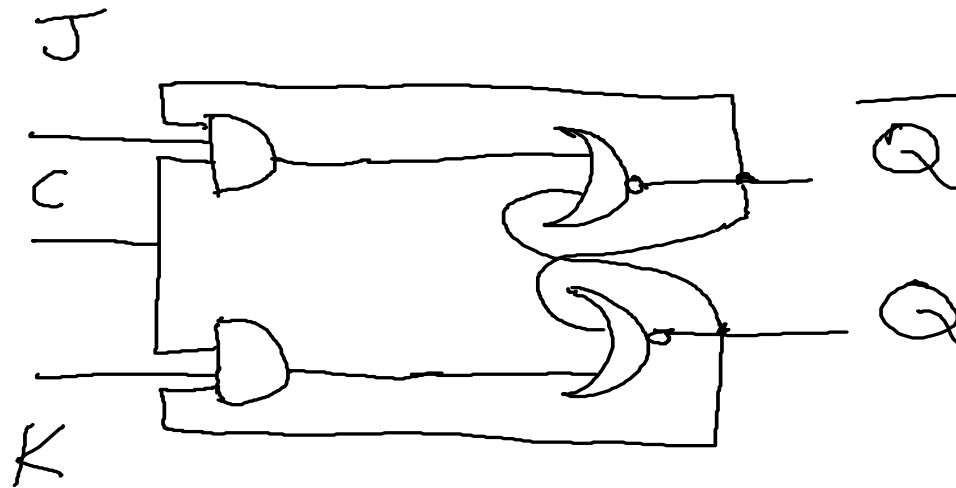 - add an enable (clock)

Gated SR Latch

S

C

R

$\overline{Q}$

Q

Gated SR Latch Timing Diagram
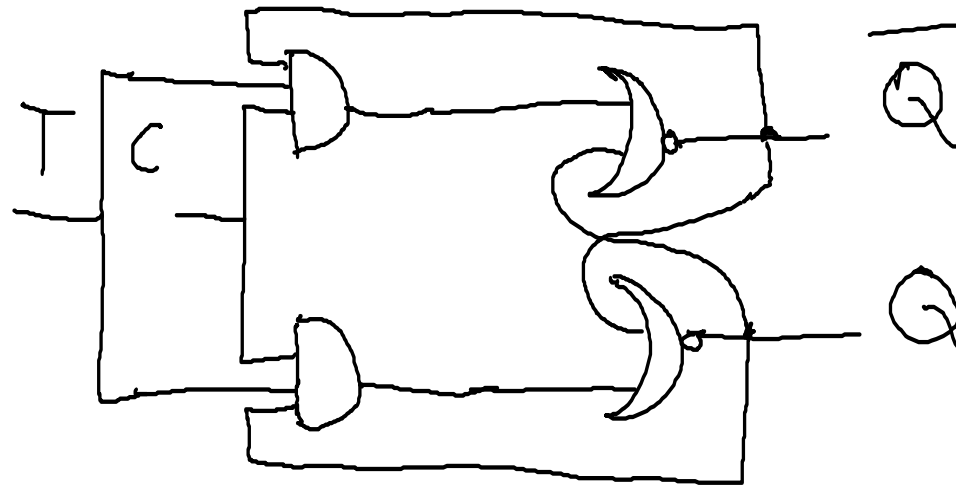

device active

C

S
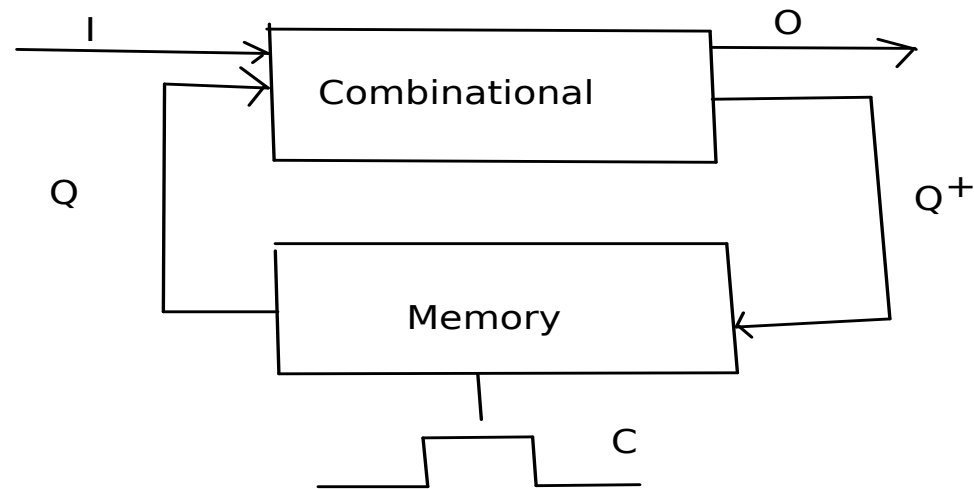
R

Q

problem

Gated D Latch

Gated JK Latch

Gated T Latch

Synchronous Sequential Systems

Gated Latches are not well suited for synchronous sequential systems because of the potential of multiple state changes per clock cycle.
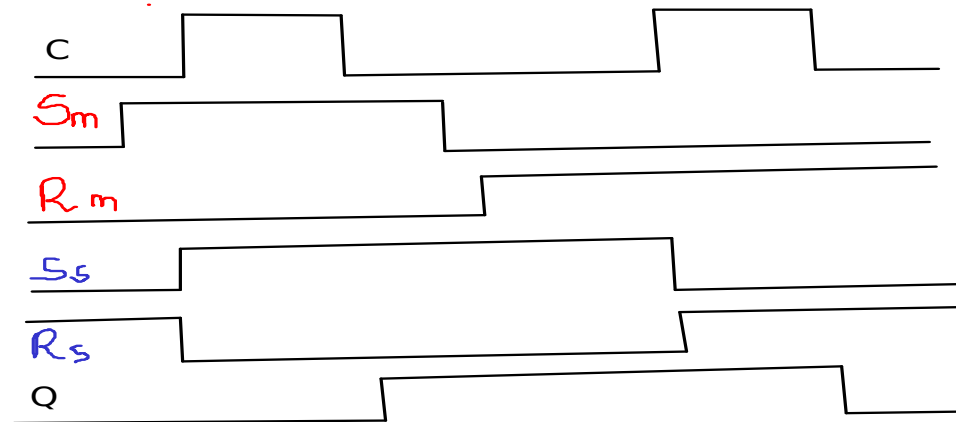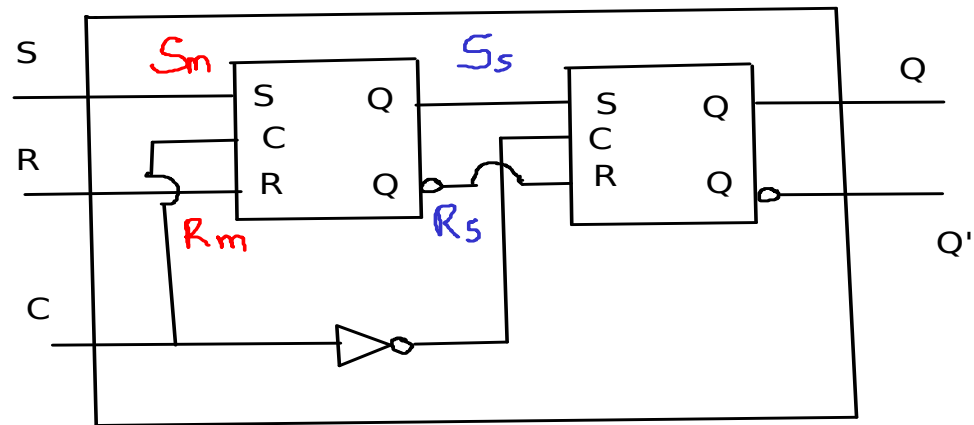
Synchronous Sequential Systems cont.

○ Inputs Change (during a clock cycle)
- • gated latch outputs are updated according
  to the appropriate characteristic equation

○ Result
- • possible multiple state changes

○ Fix
- • shorten clock pulse such that memory contents
  are only updated once per clock cycle
- • use a master-slave configuration

Master-Slave Flip Flops (FF)

○ Pulse Triggered
- • both the rising edge and the falling edge of the clock pulse are used to sample inputs and generate outputs

○ Positive Pulse Triggered
- • inputs are sampled on the falling edge
- • outputs are generated on the rising edge

○ Negative Pulse Triggered
- • inputs are sampled on the rising edge
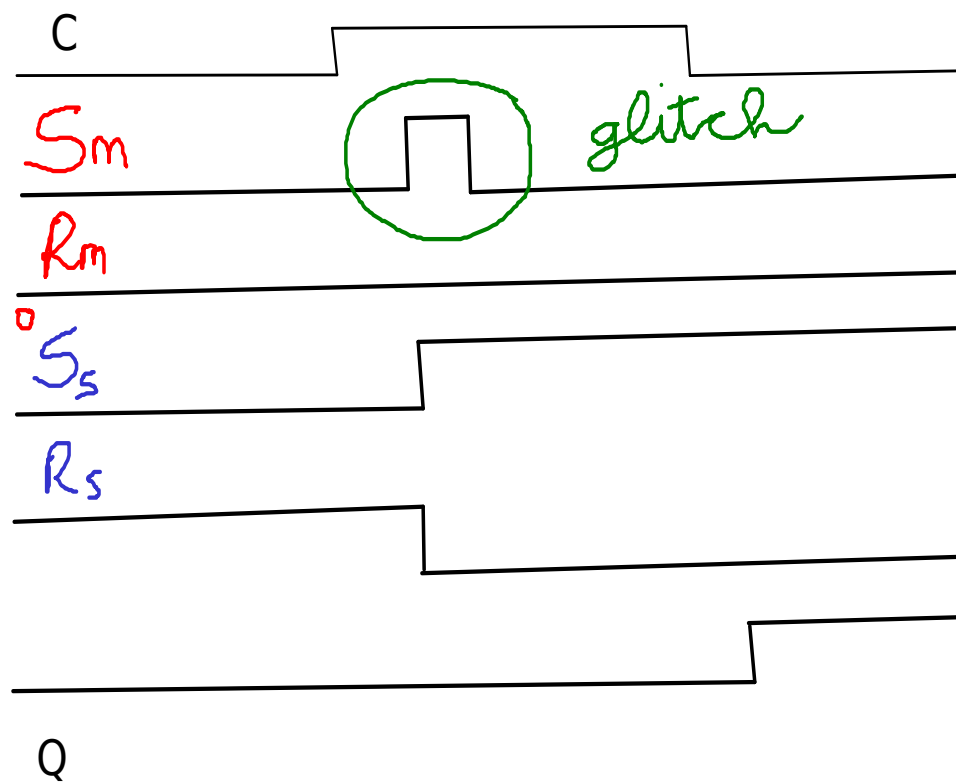- • outputs are generated on the falling edge

Negative Master-Slave FF

Negative Master-Slave FF cont.

1s Catching

C

S_m glitch

R_m

S_s

R_s

Q
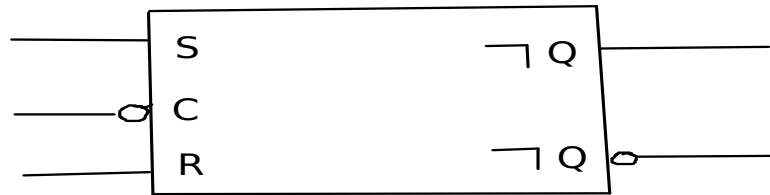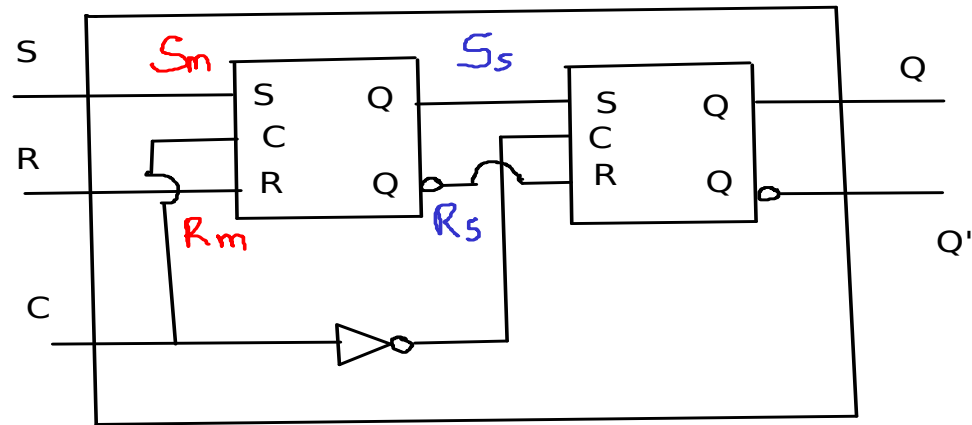
Synchronous Sequential Systems

Master Slave FFs are not well suited for synchronous sequential systems because of "wrong" single state change.

○ Problem
- when the master is enabled, a glitch can incorrectly set/reset the master output (slave input)

○ Fix
- remove hazards
- move to edge-triggered devices