

Experiment 6

Consider the component declaration for a memory device called `lab6` given in `~csci355/Lab6/tb.cew`.

The modeled device is a zero-delay SR single-bit memory comprising an SR latch, an SR gated latch with an active-high enable `C`, a negative master-slave SR flip flop with a clock `C` and a positive edge-triggered SR flip flop with a clock `C`. There are four outputs, one for each of the modeled SR latches/flip flops.

Task: Identify which of `w`, `x`, `y` and `z` corresponds to the `Q` (state) output of the four modeled SR latches/flip flops. To this end, develop a testbench that can discriminate between the four SR latches/flip flops.

For the master-slave device, design a test case that will demonstrate the phenomenon of ones catching (you may assume a `nor` gate realization).

Deliverable (D1): Electronic submission of testbench source code (`make submit`) and an explanation of your testing strategy in the form of annotated timing diagrams.

Task: Design a negative master-slave SR flip flop using `nor` gates and `and` gates.

Deliverable (D2): Logic schematic.

Task: Design a TTL-based physical design for the negative master-slave SR flip flop.

Deliverable (D3): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D4): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D5): A physical realization of a negative master-slave SR flip flop that behaves

to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Note In addition to demonstrating the *normal* behaviour of your circuit to the instructor, you must also demonstrate the phenomenon of ones catching using the test-case developed in conjunction with deliverable D1.

Task: Document any relevant results, explanations or comments.

Deliverable (D6): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES