Experiment 4

Consider again the combinational system (LED Driver) and the seven segment display (LED Display) from Experiment 3. The LED Driver takes as input, a four bit binary number (`w,x,y,z` with `z` the LSB) and produces active low output to drive the LED Display. For this experiment, if the input is between `0000` and `1001` inclusive then the LED Display's segments `a` through `g` are illuminated so as to display the decimal character that represents the input.[2] The LED Display's decimal point `dp` is NOT illuminated. See the testbench in `csci355/Lab4` to determine the exact segment pattern for each decimal digit.

Task: Perform problem analysis.

Deliverable (D1): Truth table for the LED Driver with one output column for each of `a, b, c, d, e, f, g` and `dp`.

Task: Design a ROM to implement the LED Driver. Use a decoder and `nand`/`or` gate(s) to implement the ROM.

Deliverable (D2): Logic schematic for the LED Driver.

Task: Develop a structural Verilog model of the LED Driver using the Verilog models for the TTL ICs SN7432, SN7410, SN7413 and SN74154. Note, you can use two instances of SN7410.

Deliverable (D3): Electronic submission of source code (`make submit`).

Task: Map your Verilog model to an IC-based physical design using TTL components and one TIL 729 and a resistor pack (see Appendix A).

Deliverable (D4): IC logic schematic.

Task: Specify IC interconnections.

[2] illuminated means the associated input signal is asserted (active low)

Deliverable (D5): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D6): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: In the laboratory, download your physical designs to the xsa-50 FPGA board, verify its behaviour and sign-off on the design/implementation.

Deliverable (D7): A physical FPGA realization of the combinational system that behaves to specification. A hardcopy of `lab4.ucf` (file detailing FPGA area contaraints and I/O pin assignments). Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D8): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES