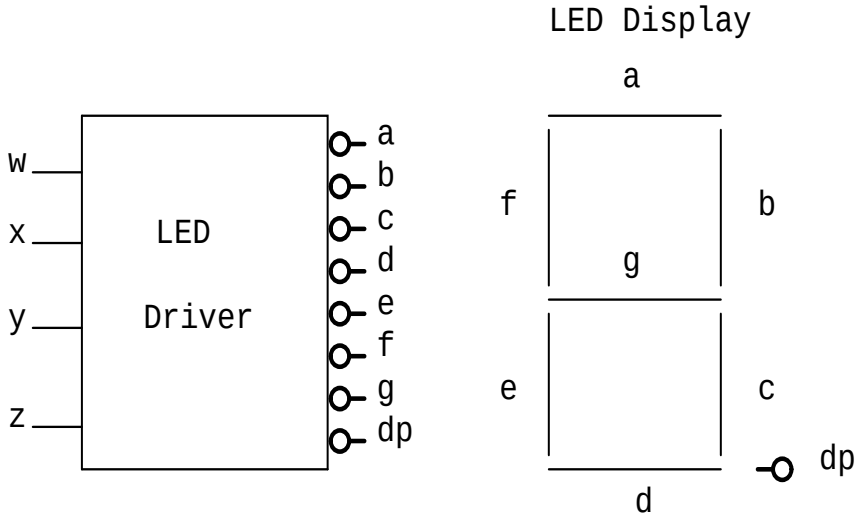
Experiment 3

A seven segment display is used to display a decimal digit (or a hex digit). Such displays are often found in electronic watches, clocks and appliances. The seven segment display used in this lab consists of seven LED segments and a decimal point (see Appendix A, TIL 729).

Consider the combinational system (LED Driver) and the seven segment display (LED Display) depicted in the following logic schematic:



The LED Driver takes as input, a four bit binary number (`w,x,y,z` with `z` the LSB) and produces active low output to drive the LED Display. If the input is between `0000` and `1001` inclusive then the LED Display's decimal point `dp` is illuminated.[1] If the input is between `1010` and `1111` inclusive then the LED Display's decimal point `dp` is not illuminated and the LED Display's segments `a` through `g` are illuminated so as to display the hex character (in upper case) that represents the input. For example, if the input is `1111` then the segments `a`, `e`, `f` and `g` are illuminated. All other segments (including the decimal point `dp`) are not illuminated.

Task: Perform problem analysis.

[1] illuminated means the associated input signal is asserted (active low)

Deliverable (D1): Truth table for the LED Driver with one output column for each of `a, b, c, d, e, f, g` and `dp`.

Task: Use espresso to derive a minimized SOP expression for the LED Driver.

Deliverable (D2): Hardcopy of espresso output.

Task: Perform symbolic analysis.

Deliverable (D3): Logic schematic derived from espresso output and a network expression specifying LED driver output in terms of its inputs.

Task: Develop a structural Verilog model of the LED Driver using the Verilog models for the TTL ICs SN7432, SN7408, SN7411 and SN7404.

Deliverable (D4): Electronic submission of source code (`make submit`).

Task: Map your Verilog model to an IC-based physical design using TTL components and one TIL 729 and a resistor pack (see Appendix A).

Deliverable (D5): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D6): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D7): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: In the laboratory, download your physical designs to the xsa-50 FPGA board, verify its behaviour and sign-off on the design/implementation.

Deliverable (D8): A physical FPGA realization of the combinational system that behaves to specification. A hardcopy of `lab3.ucf` (file detailing FPGA area contaraints and I/O pin assignments). Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D9): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES