

## Experiment 2

With reference to the Verilog description in `/Lab2/lab2.v`:

**Task:** Extract the IC logic schematic from the Verilog description.

**Deliverable (D1):** IC logic schematic.

**Task:** Extract the combinational logic schematic.

**Deliverable (D2):** Logic schematic.

**Task:** Perform symbolic analysis.

**Deliverable (D3):** Network expression specifying the output in terms of its inputs.

**Task:** Perform literal analysis.

**Deliverable (D4):** Truth table with one output column for each of I1, I2, I3, I4 and E.

**Task:** Derive a minimal SOP expression for the modeled circuit.

**Deliverable (D5):** A listing of all the prime-implicants, the essential prime-implicants and the secondary prime-implicants. A minimal SOP expression and a K-Map showing the corresponding implicant cover.

**Task:** Develop a testbench for the modeled circuit. You must use a gold function as exemplified in the testing of SN7400. You must use your minimal SOP expression as the gold function.

**Deliverable (D6):** Electronic submission of source code (`make submit`).

**Task:** Specify IC interconnections.

**Deliverable (D7):** One completed pin-out sheet (at least) for each IC employed in the physical design.

**Task:** In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

**Deliverable (D8):** A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

**Task:** Document any relevant results, explanations or comments.

**Deliverable (D9):** A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

## NOTES