CSCI 355 Digital Logic and Computer Organization

Laboratory Manual

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1. Preamble

CSCI 355 is concerned with the analysis and design of digital circuits. Two methods of design verification are employed. First, a software model of the design is developed and tested using the hardware description language Verilog. Then, the design is physically realized and tested in the laboratory.

Design modeling using Verilog is discussed in the lecture portion of this course. Models are developed for simulation and for synthesis. Designs are realized either on a breadboard using standard ICs (integrated circuits) or on a XSA-50 FPGA based prototyping board.

Breadboarding and the XSA-50 board are overviewed in sections 2 and 3 respectively. Section 4 discusses experiment deliverables. The remainder of the manual contains a series of laboratory tasks (experiments) and data sheet appendices.

2. Breadboarding

During breadboarding, you will plug the necessary ICs into the breadboard, cut wires of proper length, and connect the ICs on the breadboard using the wires according to your design specification (schematic). At the end of this section, a tutorial from Hobby Electronics introduces basic breadboarding (`http://www.hobby-electronics.com/MiniTutorialIndex.htm`). The following descriptions assume you have read and understood the tutorial.

IDL-800 Digital Circuit Evaluator

Our laboratory is equipped with IDL-800 digital circuit evaluators. The IDL-800 has 19 different basic components. Initially, you will be concerned with the following 6 components:

1 power switch with indicator

2 pulse switches

3 level switches

4 removable solderless breadboard

5 fixed DC +5volts and ground

6 leds (lamps)

IDL-800 Digital Circuit Evaluator

Wiring Technique

It is important to develop good wiring technique when realizing your designs on a breadboard. Good wiring technique will help both the student and the instructor test and debug your circuit realization. The following convention must be adhered to:

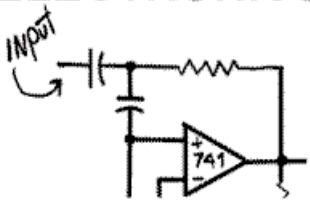
- Power to the IDL-800 should be off before you insert or remove wires or ICs from the unit.
- Insert your required ICs into the breadboard gap as described in the tutorial. Note that ICs have a notch that is used as an alignment reference. ICs have legs or pins that are the input/output interface to the circuits on the chip. The legs bend easily, you may have to align them (straighten them) before inserting the IC in the breadboard gap. Make sure adjacent IC legs are inserted into adjacent breadboard pin-holes. To achieve correct IC orientation, the two rows of IC legs must straddle the breadboard gap and the IC notch must be on the left hand side of the IC.
- To remove an IC from the breadboard, slide an IC chip extractor under the body of the chip and lift gently (a pencil will work if you dont have an extractor to hand).
- Cut wires to the appropriate length. Route wires around, not over ICs. Whenever possible, make manhatten (90 degree) wiring turns along unoccupied sections of the breadboard. Colour code your wires. Use red for +5volts, black for ground, green for data signals and blue for control signals. Use the rails to supply +5 and ground signals to the ICs.

The following wiring sequence is strongly recommended:

- wire the +5volts and ground rails
- wire the +5volts and ground signals (from the rails to the ICs)
- wire data signals
- wire control signals

One final note, on occasion, you may end up using an IC that is faulty. Consequently, it is strongly recommended that you verify the operation of each IC in isolation BEFORE you wire-up your circuit.

hobby ELECTRONICS



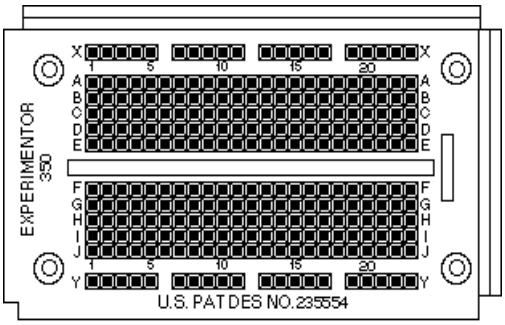
Breadboarding Basics

Home

Mini-Tutorial Index

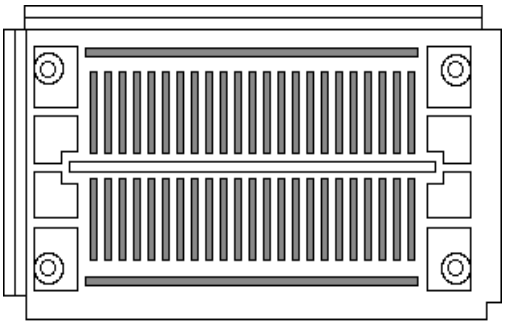
The best method of experimenting with ICs is to use a "breadboard" to build circuits. Breadboards, more formally known as *solderless modular sockets*, get their name from the early days of radio, when it was common to build vacuum tube circuit prototypes on a wooden breadboard.

Today's breadboards are a grid of insulating plastic atop a pattern of conducting metal strips. Here is a top view of a typical breadboard:



Component leads and wires are inserted into the holes and make contact with the conducting metal strips underneath, thus "connecting" them together.

The pattern of conducting strips underneath the insulating plastic is shown below. Notice there are two horizontal strips along both sides of the breadboard and a series of shorter vertical strips. The two horizontal strips are normally used for power supply connections, with one strip being the supply voltage and the other being the ground connection. (Breadboards with four horizontal strips are available, and are used for circuits requiring dual polarity or multiple voltage power supplies.) The horizontal strips are often known as *rails*.



Note the gap separating the vertical strips. The dual in-line package (DIP) IC is normally

placed across this gap. One row of pins is one side of the gap, and the other row of pins is on the opposite side.

Breadboards come in a variety of sizes, and are usually measured in terms of the number of connection or "tie points" provided. Some breadboards come with binding posts for connecting a power supply; deluxe models have power supplies built in and with additional supports for potentiometers, LEDs, and meters.

3. XSA-50 Prototyping Board

The Xess XSA-50 prototyping board contains a Xilinx Spartin II FPGA with 50,000 gates (the board's manual is linked off the CSCI 355 course page). The FPGA can be programmed in-the-lab to execute a circuit synthesized from a Verilog model. The FPGA programming process is similar to downloading an S19 record file to a HC11 development board. The "object" code file is called a bit-file and has a `.bit` file-name extension. The XSTOOLS form Xess interface the development environment with the board through a connecting parallel port. The tools allow for board testing (`xstest`); bit-file downloading (`xsload`) and I/O (`xsport`). With regard to I/O, certain FPGA input-pins and 7-segment LED output-pins are mapped to pins in the parallel port. The I/O mappings are given below (see Appendix A for LED segment labels):

port bit	6	5	4	3	2	1	0
pin	58	51	65	47	42	48	50

LED	a	b	c	d	e	f	g	dp
pin	49	46	39	67	62	57	60	44

Note, the most significant bit of the parallel port is also mapped but it is recommended that it always be set. The following annotated command sequence demonstrates how to download and exercise a two-input one-output logical AND gate. The inputs are mapped to port-pins 0 and 1 and, the output is mapped to LED segment *c*.

```
xstest -b xsa-50       -- test the xsa-50 board
xsload -fpga and2.bit  -- download and2.bit to the board
xsport 10000011        -- port-bit 0 and port-bit 1 are asserted (assume positive logic)
```

XSA-50

Price: $59.00
In Stock: Yes

Features:

- XC2S50 FPGA
- XC9572XL CPLD
- 8 MByte SDRAM
- 128 KByte Flash
- 100 MHz programmable oscillator
- Parallel port
- Keyboard/mouse PS/2 port
- 64-color VGA port
- 7-segment LED
- 1 pushbutton
- 4 DIP switches
- 84-pin prototyping interface (53 I/O pins)
- 5V-tolerant I/O
- 9V DC power jack
- 5V / 3.3V / 2.5V regulators
- Downloading cable
- XSTOOLs utilities CDROM
- Works with the XST-3.0 Board
- Works with XILINX ISE, WebPACK, iMPACT and ChipScope software

Documentation:

- XSA-50 Board Manual (PDF file)
- XSA-50 Board Pin List (Excel file)

Accessories:

- XStend Board 3.0
- 9 VDC power supply (North America)
- 9 VDC power supply (Europe)

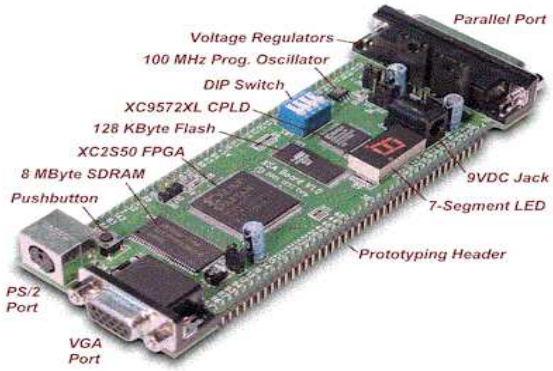
The XSA-50 Board keeps the same form-factor as our popular XS40 Boards while increasing the logic density to 50,000 gates with a Spartan-2 XC2S50 FPGA. The FPGA is combined with a 8 MByte synchronous DRAM and 128 KByte Flash to give you the resources for building a complete, soft-core RISC microcontroller system! Or anything else you might think of...

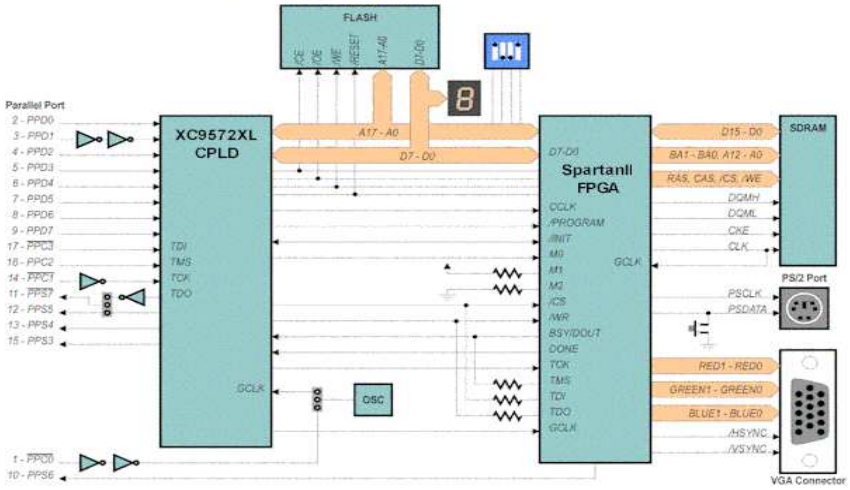
The bitstream for the XSA-50 can be stored in the on-board 128 KByte Flash so the FPGA loads its configuration as soon as power is applied. Or you can download directly to the board through the parallel port with the XSTOOLs utilities we provide. The interface CPLD on the XSA-50 also supports downloading with XILINX iMPACT and circuit test/debug with ChipScope software using our simple downloading cable. No more expensive XILINX cables!

In addition to the large FPGA, SDRAM and Flash chips, you also get a VGA port that produces vivid graphics in 64 colors. And the prototyping header gives you 53 general-purpose I/O pins for building interfaces to external devices.

And the XSA-50 helps you maintain your investment. Use your existing XStend Boards to add a stereo codec, LEDs, switches, and a dedicated prototyping area to the XSA-50. And keep your power supplies - the XSA-50 has the same power connections as an XS40 Board.

Think it will be a big switch to move from the XS40 Boards to the XSA-50? Well, we provide all the software utilities for programming the FPGA, setting the oscillator frequency, and downloading and uploading the RAM and Flash. And we make all the source code available for you to play with! How about design examples? We have parameterized modules for interfacing to the PS/2 keyboard port, displaying images through the VGA port, and reading/writing to the synchronous DRAM as if it were a simple static RAM. And we will be adapting all the chapters of our Pragmatic Logic Design online text to support the XSA-50.





4. Experiment Deliverables and Evaluation

The remainder of the manual contains a series of laboratory tasks (experiments). Each experiment has a pre-lab component and an in-lab component. In the pre-lab component, you develop solution(s) to the laboratory task(s) and verify your design(s) by building and testing Verilog model(s). All files relating to laboratory work can be found in `otter:~pwalsh/csci355`. For Lab$x$, the design file and the design testbench can be found in `otter:~pwalsh/csci355/Labs/Lab`x. Models for `sn74??` TTL ICs can be found in `otter:~pwalsh/csci355/Labs`.

In the in-lab component, your task is to realize your circuit design(s), verify them and record any relevant observations you made during the in-lab period.

Pre-lab Verilog code is due before 12:00 noon on the day BEFORE your scheduled in-lab time. If your model(s) fail any of the supplied test cases (in the testbench(s)) then you will not be allowed to proceed to the in-lab component. You will receive no credit for the experiment.

You must complete a experiment report for each laboratory task. The report is due at the beginning of your in-lab time; all report deliverables must be in place with the exception of deliverables that are due by the end of your in-lab time. Your report will be initialed by the instructor and returned to you for the duration of the in-lab time. Once you have constructed and verified the behaviour of your circuit, sign your report to indicate your circuit behaves as specified. Then, ask your instructor to check your work. If either your design or implementation if found to be flawed, you will receive no credit for the physical realization component of the experiment. Submit the complete report to your instructor at the end of the in-lab time.

Each Lab is graded out of 100 points. The breakdown is as follows:

- **10 points:** report presentation

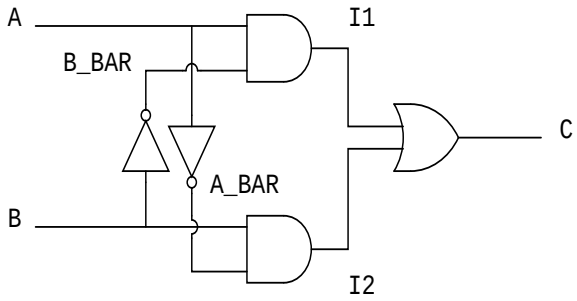
- **45 points:** report deliverables
- **45 points:** physical circuit behaviour

A sample report follows the statement of Lab0. All pages of your report must be stapled together. All pages of your report must have a page number on the top right hand corner in the form of `Page n of m`. You need not word-process your reports but hand drawn figures and writing must be clear and legible.

The exact wiring connections for your circuit must be detailed in pin-out sheets. You must complete at least one pin-out sheet for each IC employed in your physical circuit. For a given IC, each row in its pin-out sheet details a wire connecting one of its pins to another pin on the same IC or to a pin on a different IC. Consider wire `X`. Let the the source and destination of wire `X` be called `A` and `B`. When the pin-out is done correctly, you will find that `X`'s connection details are listed at least twice; first detailing the connection from `A` to `B` and then detailing the connection from `B` to `A`. At the end of a pin-out sheet, you may repeat *significant* connections such as connections to switches and leds. You must use the pin-out sheet template for all pin-outs.

Experiment 0

With reference to the combinational system specified in the following logic schematic:



Task: Perform symbolic analysis.

Deliverable (D1): Network expression specifying `C` in terms of `A` and `B`.

Task: Perform literal analysis.

Deliverable (D2): Truth table with one output column for each of `A_BAR, B_BAR, I1, I2` and `C`.

Task: Develop a sinthesizable structural Verilog model of the combinational system using the Verilog models for the TTL ICs sn7404, sn7408 and sn7432.

Deliverable (D3): Electronic submission of source code (`make submit`).

Task: Map your Verilog model to a TTL-based physical design for the combinational system.

Deliverable (D4): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D5): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D6): A physical bread-board realization of the combinational system that be-

haves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: In the laboratory, download your physical designs to the xsa-50 FPGA board, verify its behaviour and sign-off on the design/implementation.

Deliverable (D7): A physical FPGA realization of the combinational system that behaves to specification. A hardcopy of `lab0.ucf` (file detailing FPGA area contaraints and I/O pin assignments). Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D8): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES

Experiment 0 Report: Page 1 of 6

CSCI 355

Experiment 0 Report

Peter Walsh (Lab Section F0001)

Deliverable D1

$$C = \texttt{A}\overline{\texttt{B}} + \overline{\texttt{A}}\texttt{B}$$

Deliverable D2

A	B	A_BAR	B_BAR	I1	I2	C
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

Deliverable D3

Submitted electronically through `make submit`.

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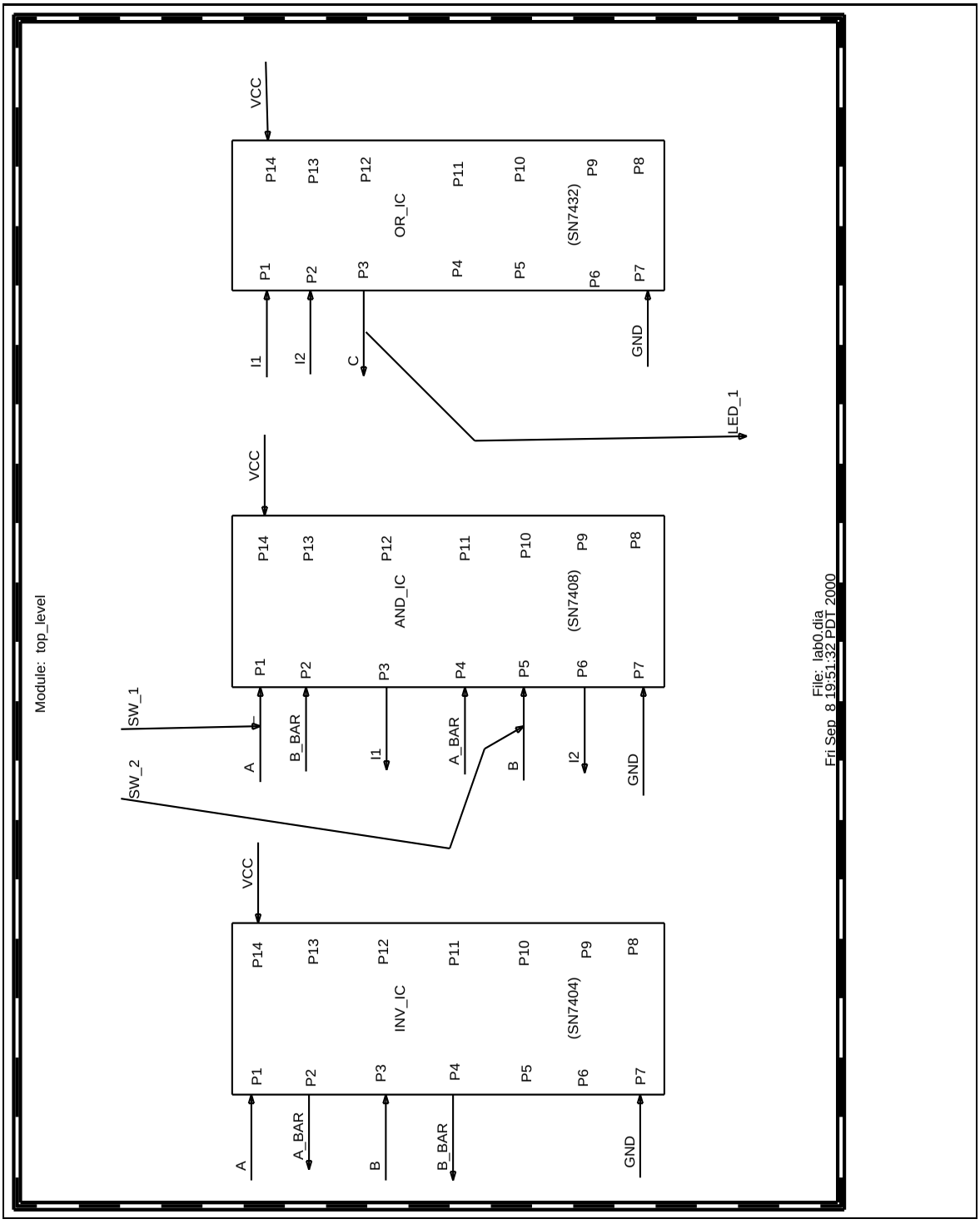
Deliverable D4



Deliverable D5

CSCI 355 Laboratory Pin-Out Sheet

STUDENT NAME Peter W Page__3____Of__6____

EXPERIMENT NUMBER 0

IC NUMBER SN7432

IC INSTANCE NAME OR_IC

Source		*Destination*	
Pin Number	VHDL Alias Name (optional)	Pin Number	VHDL Alias Name (optional)
P1	A1	AND_IC.P3	Y1
P2	B1	AND_IC.P6	Y2
P3	Y1	LED_1	
P7	GND	+0V	
P14	VCC	+5V	
LED_1		OR_IC.P3	Y1

CSCI 355 Laboratory Pin-Out Sheet

STUDENT NAME Peter W Page__4____Of__6____

EXPERIMENT NUMBER 0

IC NUMBER SN7408

IC INSTANCE NAME AND_IC

Source		*Destination*	
Pin Number	VHDL Alias Name (optional)	Pin Number	VHDL Alias Name (optional)
P1	A1	INV_IC.P1	A1
		SW_1	
P2	B1	INV_IC.P4	Y2
P3	Y1	OR_IC.P1	A1
P4	A2	INV_IC.P2	Y1
P5	B2	INV_IC.P3	A2
		SW_2	
P6	Y2	OR_IC.P2	B1
P7	GND	+0V	
P14	VCC	+5V	
SW_1		AND_IC.P1	A1
SW_2		AND_IC.P5	B2

CSCI 355 Laboratory Pin-Out Sheet

STUDENT NAME Peter W Page__5____Of__6____

EXPERIMENT NUMBER 0

IC NUMBER SN7404

IC INSTANCE NAME INV_IC

Source		*Destination*	
Pin Number	VHDL Alias Name (optional)	Pin Number	VHDL Alias Name (optional)
P1	A1	AND_IC.P1	A1
P2	Y1	AND_IC.P4	A2
P3	A2	AND_IC.P5	B2
P4	Y2	AND_IC.P2	B1
P7	GND	+0V	
P14	VCC	+5V	

Experiment 0 Report: Page 6 of 6

Deliverable D6

Exhaustive testing (all 4 input test patterns) was employed. The physical system (bread-board) behaved as specified. `Signature:` *Peter W*

Deliverable D7

```
#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments

NET "A"  LOC = "P50"  ;

NET "B"  LOC = "P48"  ;

NET "C"  LOC = "P44"  ;

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE
```

Exhaustive testing (all 4 input test patterns) was employed. The physical system (FPGA) behaved as specified. `Signature:` *Peter W*

Deliverable D8

Results/Explanations/Comments:

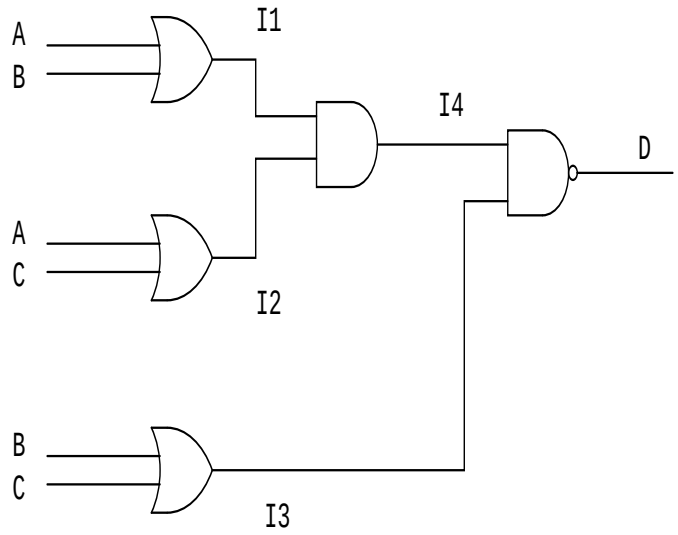
Nothing further to report.

`<<<<<<<<<<<< End of Report >>>>>>>>>>>>`

Photographs of physical realizations of the circuit from Experiment 0 can be accessed from the csci 355 course web page.

Experiment 1

With reference to the combinational system specified in the following logic schematic:



Task: Perform symbolic analysis.

Deliverable (D1): Network expression specifying `D` in terms of `A`, `B` and `C`.

Task: Perform literal analysis.

Deliverable (D2): Truth table with one output column for each of `I1, I2, I3, I4` and `D`.

Task: Develop a structural Verilog model of the combinational system using the Verilog models for the TTL ICs sn7432, sn7408 and sn7400.

Deliverable (D3): Electronic submission of source code (`make submit`).

Task: Map your Verilog model to a TTL-based physical design for the combinational system.

Deliverable (D4): IC logic schematic.

Task: Specify IC interconnections.

Deliverable (D5): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task: In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D6): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: In the laboratory, download your physical designs to the xsa-50 FPGA board, verify its behaviour and sign-off on the design/implementation.

Deliverable (D7): A physical FPGA realization of the combinational system that behaves to specification. A hardcopy of `lab1.ucf` (file detailing FPGA area contaraints and I/O pin assignments). Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task: Document any relevant results, explanations or comments.

Deliverable (D8): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES